

SPECIFICATIONS

PCI-5122

100 MHz, 100 MS/s, 14-Bit PCI Oscilloscope Device

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Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured* specifications describe the measured performance of a representative model.

Specifications are *Typical* unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All filter settings
- All impedance selections
- Sample clock set to 100 MS/s

Vertical

Analog Input

Number of channels	Two (simultaneously sampled)
Connectors	BNC

Impedance and Coupling

Input impedance (software-selectable)	50 Ω \pm 2.0% 1 M Ω \pm 0.75% in parallel with a nominal capacitance of 29 pF
Input coupling (software-selectable)	AC ¹ DC GND

Voltage Levels

Table 1. Full Scale (FS) Input Range and Programmable Vertical Offset

Range (V _{pk-pk})	Vertical Offset Range	
	50 Ω Input	1 M Ω Input
0.2 V	\pm 0.1 V	
0.4 V	\pm 0.2 V	
1 V	\pm 0.5 V	
2 V	\pm 1 V	
4 V	\pm 2 V	
10 V	—	\pm 5 V
20 V (1 M Ω only)	—	—

Maximum input overload

50 Ω	7 V _{rms} with Peaks \leq 10 V
1 M Ω	Peaks \leq 42 V

Accuracy

Resolution	14 bits
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¹ AC coupling available on 1 M Ω input only.

Table 2. DC Accuracy², Warranted

Input Range (V_{pk-pk})	DC Accuracy
0.2 V and 0.4 V	$\pm(0.65\%$ of input + 1.0 mV)
1 V	$\pm(0.65\%$ of input + 1.2 mV)
2 V	$\pm(0.65\%$ of input + 1.6 mV)
4 V and 10 V	$\pm(0.65\%$ of input + 8.0 mV)
20 V (1 M Ω only)	$\pm(0.65\%$ of input + 13.0 mV)

Programmable vertical offset accuracy³ $\pm 0.5\%$ of offset setting, Warranted

Table 3. DC Drift, nominal

Input Range (V_{pk-pk})	50 Ω and 1 M Ω
0.2 V, 0.4 V, 1 V, and 2 V	$\pm(0.057\%$ of input + 0.006% of FS + 100 μ V) per $^{\circ}$ C
4 V, 10 V	$\pm(0.057\%$ of input + 0.006% of FS + 900 μ V) per $^{\circ}$ C
20 V (1 M Ω only)	

AC amplitude accuracy

50 Ω	± 0.06 dB ($\pm 0.7\%$) at 50 kHz
1 M Ω	± 0.09 dB ($\pm 1.0\%$) at 50 kHz

Crosstalk⁴ ≤ -100 dB at 10 MHz

Bandwidth and Transient Response

Bandwidth (± 3 dB)⁵

0.2 V input range	80 MHz up to 40 $^{\circ}$ C, ⁶ warranted
All other input ranges	100 MHz, warranted

² Programmable vertical offset = 0 V. Within ± 5 $^{\circ}$ C of self-calibration temperature.

³ Within ± 5 $^{\circ}$ C of self-calibration temperature.

⁴ CH 0 to/from CH 1 and External Trigger to CH 0 or CH 1.

⁵ Filters off.

⁶ 78 MHz above 40 $^{\circ}$ C.

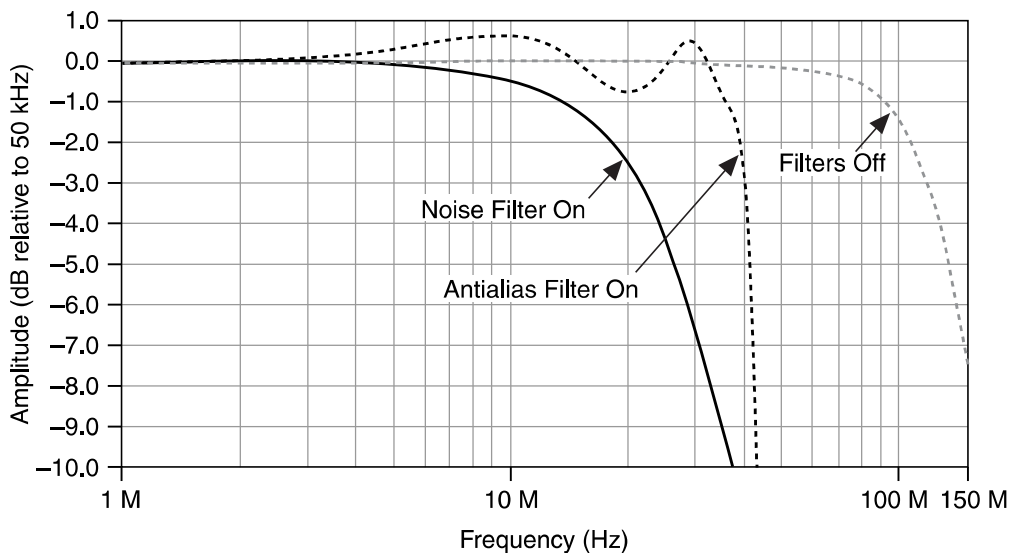
Rise/fall time

0.2 V input range	4.2 ns
All other input ranges	3.5 ns
Bandwidth limit filters⁷	
Noise filter (2-pole Bessel)	20 MHz
Anti-alias filter (6-pole Chebyshev)	40 MHz (-6 dB) 35 MHz (± 3 dB), warranted
AC coupling cutoff (-3 dB)⁸	12 Hz

Table 4. Passband Flatness⁹

Filter Settings	Input Range (V_{pk-pk})	50 Ω and 1 M Ω
Filters off	0.2 V	± 0.4 dB (DC to 20 MHz) ± 1 dB (20 MHz to 40 MHz)
	All other input ranges	± 0.4 dB (DC to 20 MHz) ± 1.0 dB (20 MHz to 50 MHz)
Anti-alias filter on	All ranges	± 1.2 dB (DC to 16 MHz) ± 1.6 dB (16 MHz to 32 MHz)

Figure 1. PXIe-5122 Frequency Response, Measured



⁷ Only one filter can be enabled at any given time. The anti-alias filter is enabled by default.

⁸ AC coupling available on 1 M Ω input only.

⁹ Referenced to 50 kHz.

Spectral Characteristics

Table 5. Spurious-Free Dynamic Range with Harmonics (SFDR)¹⁰

Range (V_{pk-pk})	50 Ω	1 M Ω
0.2 V	75 dBc	70 dBc
0.4 V	75 dBc	70 dBc
1 V	75 dBc	70 dBc
2 V	75 dBc	70 dBc
4 V	65 dBc	70 dBc
10 V	65 dBc	60 dBc
20 V	—	60 dBc

Table 6. Total Harmonic Distortion (THD)¹¹

Range (V_{pk-pk})	50 Ω	1 M Ω
0.2 V	-75 dBc	-68 dBc
0.4 V	-75 dBc	-68 dBc
1 V	-75 dBc	-68 dBc
2 V	-73 dBc	-68 dBc
4 V	-63 dBc	-68 dBc
10 V	-63 dBc	-58 dBc
20 V	—	-58 dBc

Intermodulation distortion¹²

-75 dBc

¹⁰ 10 MHz, -1 dBFS input signal. Includes the 2nd through the 5th harmonics. Measured from DC to 50 MHz.

¹¹ 10 MHz, -1 dBFS input signal. Includes the 2nd through the 5th harmonics.

¹² 0.2 V to 2.0 V input range. 50 Ω input impedance. Two tones at 10.2 MHz and 11.2 MHz. Each tone is -7 dBFS.

Table 7. Signal-to-Noise Ratio (SNR)¹³

Range (V _{pk-pk})	50 Ω		1 MΩ	
	Filters Off	Anti-alias Filter On	Filters Off	Anti-alias Filter On
0.2 V	60 dB	60 dB	56 dB	60 dB
0.4 V	62 dB	62 dB	61 dB	62 dB
1 V	62 dB	62 dB	62 dB	62 dB
2 V	62 dB	62 dB	62 dB	62 dB
4 V	—	—	61 dB	62 dB

Table 8. Signal to Noise and Distortion (SINAD)¹⁴

Range (V _{pk-pk})	50 Ω		1 MΩ	
	Filters Off	Anti-alias Filter On	Filters Off	Anti-alias Filter On
0.2 V	60 dB	60 dB	56 dB	59 dB
0.4 V	62 dB	62 dB	60 dB	61 dB
1 V	62 dB	62 dB	61 dB	61 dB
2 V	62 dB	62 dB	61 dB	61 dB
4 V	—	—	60 dB	61 dB

¹³ 10 MHz, -1 dBFS input signal. Excludes harmonics. Measured from DC to 50 MHz.

¹⁴ 10 MHz, -1 dBFS input signal. Includes harmonics. Measured from DC to 50 MHz.

Figure 2. PXIe-5122 Dynamic Performance, 50 Ω, 1 V Range, Measured

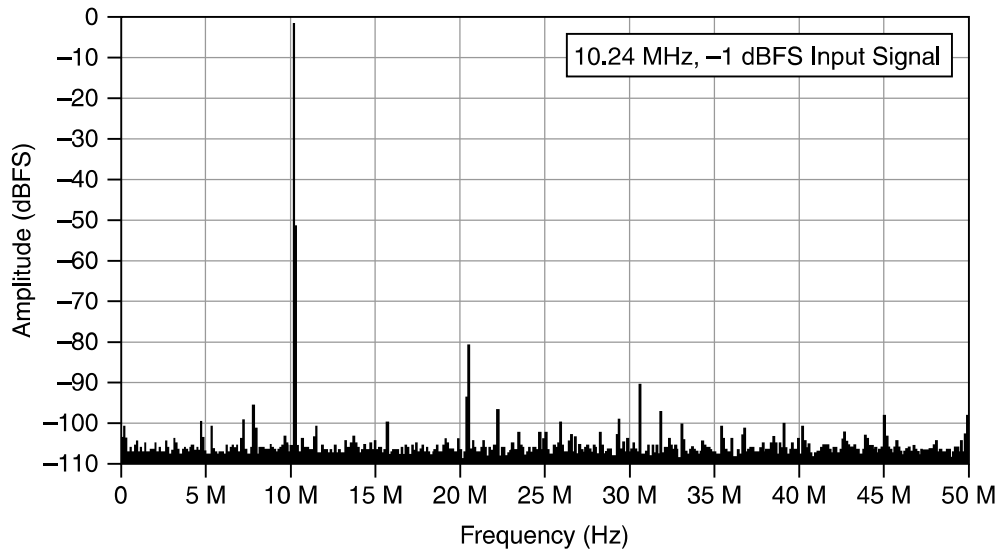


Table 9. RMS Noise (Noise Filter On)¹⁵

Range (V _{pk-pk})	50 Ω	1 MΩ
0.2 V	46 μV _{rms} (0.023% FS)	60 μV _{rms} (0.030% FS)
0.4 V	92 μV _{rms} (0.023% FS)	92 μV _{rms} (0.023% FS)
1 V	230 μV _{rms} (0.023% FS)	230 μV _{rms} (0.023% FS)
2 V	460 μV _{rms} (0.023% FS)	460 μV _{rms} (0.023% FS)
4 V	920 μV _{rms} (0.023% FS)	920 μV _{rms} (0.023% FS)
10 V	2.3 mV _{rms} (0.023% FS)	2.3 mV _{rms} (0.023% FS)
20 V	—	4.6 mV _{rms} (0.023% FS)

Table 10. RMS Noise (Anti-alias Filter On)¹⁵

Range (V _{pk-pk})	50 Ω	1 MΩ
0.2 V	66 μV _{rms} (0.033% FS)	80 μV _{rms} (0.040% FS)
0.4 V	100 μV _{rms} (0.025% FS)	120 μV _{rms} (0.030% FS)
1 V	250 μV _{rms} (0.025% FS)	300 μV _{rms} (0.030% FS)
2 V	500 μV _{rms} (0.025% FS)	600 μV _{rms} (0.030% FS)
4 V	1 mV _{rms} (0.025% FS)	1.2 mV _{rms} (0.030% FS)

¹⁵ 50 Ω terminator connected to input.

Table 10. RMS Noise (Anti-alias Filter On)¹⁵ (Continued)

Range (V _{pk-pk})	50 Ω	1 MΩ
10 V	2.5 mV _{rms} (0.025% FS)	3 mV _{rms} (0.030% FS)
20 V	—	6 mV _{rms} (0.030% FS)

Table 11. RMS Noise (Filters Off)¹⁵

Range (V _{pk-pk})	50 Ω	1 MΩ
0.2 V	66 μV _{rms} (0.033% FS)	110 μV _{rms} (0.055% FS)
0.4 V	100 μV _{rms} (0.025% FS)	160 μV _{rms} (0.040% FS)
1 V	250 μV _{rms} (0.025% FS)	300 μV _{rms} (0.030% FS)
2 V	500 μV _{rms} (0.025% FS)	600 μV _{rms} (0.030% FS)
4 V	1 mV _{rms} (0.025% FS)	1.6 mV _{rms} (0.040% FS)
10 V	2.5 mV _{rms} (0.025% FS)	3 mV _{rms} (0.030% FS)
20 V	—	6 mV _{rms} (0.030% FS)

Figure 3. PXIe-5122 Spectral Noise Density, 0.2 V Input Range, Full Bandwidth, 50 Ω Input Impedance, Nominal

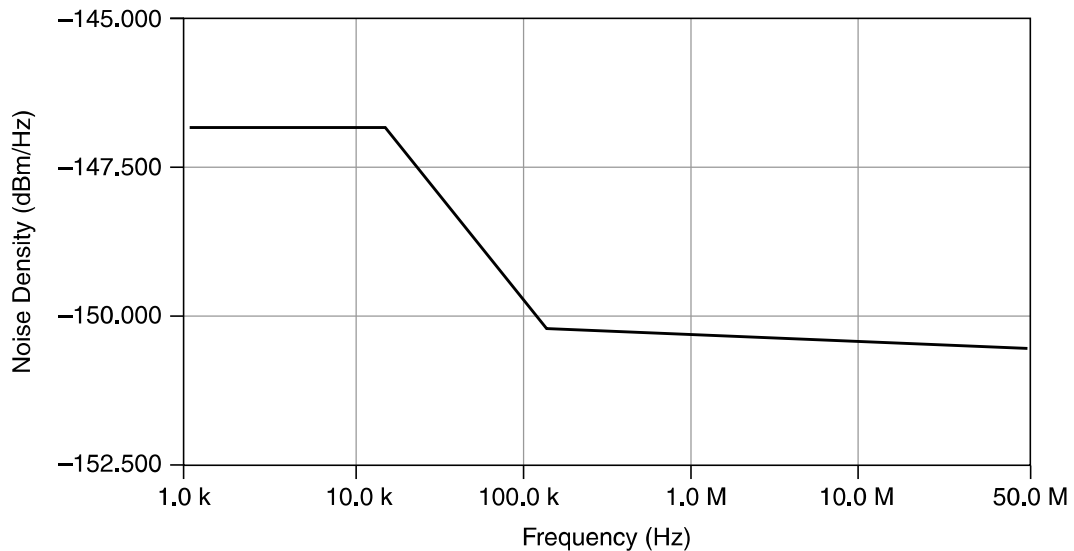
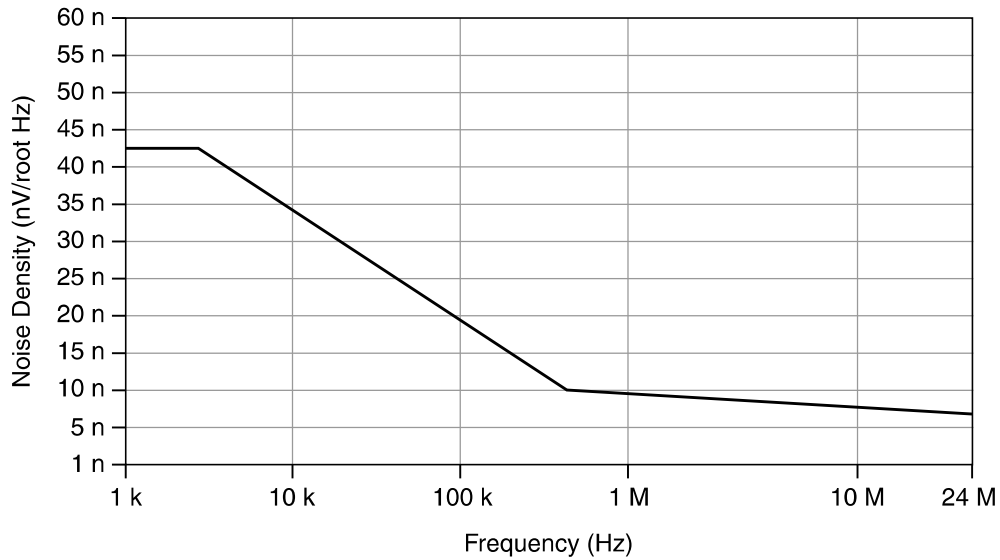


Figure 4. PXIe-5122 Spectral Noise Density, 0.2 V Input Range, Noise Filter Enabled, 1 MΩ Input Impedance, Nominal



Horizontal

Sample Clock

Sources

Internal	Onboard clock (internal VCXO) ¹⁶
External	CLK IN (front panel SMB connector) PXI Star Trigger (backplane connector)

Onboard Clock (Internal VCXO)

Sample rate range

Real-time sampling (single shot) ¹⁷	1.526 kS/s to 100 MS/s
Random interleaved sampling (RIS)	200 MS/s to 2 GS/s in multiples of 100 MS/s

Phase noise density¹⁸

<-100 dBc/Hz at 100 Hz
<-120 dBc/Hz at 1 kHz
<-130 dBc/Hz at 10 kHz

Sample clock jitter¹⁹

≤1 ps_{rms} (100 Hz to 100 kHz)
≤2 ps_{rms} (100 Hz to 1 MHz)

¹⁶ Internal Sample clock is locked to the Reference clock or derived from the onboard VCXO.

¹⁷ Divide by *n* decimation used for all rates less than 100 MS/s.

¹⁸ 10 MHz input signal.

¹⁹ Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

Timebase frequency	100 MHz
Timebase accuracy	
Not phase-locked to Reference clock	±25 ppm, Warranted
Phase-locked to Reference clock	Equal to the Reference clock accuracy
Sample clock delay range	±1 Sample clock period
Sample clock delay/adjustment resolution	≤10 ps

Related Information

For more information about Sample clock and decimation, refer to the [NI High-Speed Digitizers Help](#).

External Sample Clock

Sources	CLK IN (front panel SMB connector) PXI Star Trigger (backplane connector)
Frequency range ²⁰	30 MHz to 105 MHz (CLK IN) 30 MHz to 80 MHz (PXI Star Trigger)
Duty cycle tolerance	45% to 55%

Sample Clock Exporting

Table 12. Exported Sample Clock Destinations

Destination	Maximum Frequency
CLK OUT (front panel SMB connector)	105 MHz
PXI_Trig <0..6> (backplane connector) ²¹	20 MHz
PFI <0..1> (front panel 9-pin mini-circular DIN connector) ²¹	25 MHz
RTSI <0..6> ²¹	20 MHz

Phase-Locked Loop (PLL) Reference Clock

Sources	PXI_CLK10 (backplane connector) CLK IN (front panel SMB connector)
Frequency range ²²	5 MHz to 20 MHz in 1 MHz increments

²⁰ Divide by n decimation available, where $1 \leq n \leq 65,535$.

²¹ Decimated Sample clock only.

²² Default of 10 MHz. The PLL Reference clock frequency must be accurate to ±50 ppm.

Duty cycle tolerance	45% to 55%
Exported reference clock destinations	CLK OUT (front panel SMB connector) PFI <0..1> (front panel 9-pin mini-circular DIN connector) PXI_Trig <0..7>

CLK IN (Sample Clock and Reference Clock Input)

Connector	SMB jack
Input voltage range	
Sine wave (V_{pk-pk})	0.65 V to 2.8 V (0 dBm to 13 dBm)
Square wave (V_{pk-pk})	0.2 V to 2.8 V
Maximum input overload	$7 V_{rms}$ with $ Peaks \leq 10 V$
Impedance	50 Ω
Coupling	AC

CLK OUT (Sample Clock and Reference Clock Output)

Connector	SMB jack
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum drive current	± 48 mA

Trigger

Reference (Stop) Trigger



Note Refer to the following sections and the *NI High-Speed Digitizers Help* for more information about what sources are available for each trigger type.

Trigger types	Edge Window Hysteresis Video Digital Immediate Software
Trigger sources	CH 0 CH 1 TRIG PXI_Trig <0..6> PFI <0..1> Software
Time resolution	
Time-to-digital conversion circuit (TDC) on	
Onboard clock	100 ps
External clock	N/A
TDC off	
Onboard clock	10 ns
External clock	External clock period
Minimum rearm time ²³	
TDC on	12 μs
TDC off	3 μs
Holdoff ²⁴	
Onboard clock	Rearm time to 171.79 s
External clock	$(Rearm\ time/10\ ns) \times External\ clock\ period$ to $(2^{34} - 1) \times External\ clock\ period$

²³ Holdoff set to 0. Onboard Sample clock at maximum rate.

²⁴ TDC is off when using external Sample clock.

Analog Trigger

Trigger types	Edge Window Hysteresis
Sources	CH 0 (front panel BNC connector) CH 1 (front panel BNC connector) TRIG (front panel BNC connector)
Trigger level range	
CH 0, CH 1	100% of FS
TRIG (external trigger)	±5 V
Trigger level resolution	10 bits (1 in 1,024)
Edge trigger sensitivity	
CH 0, CH 1	2.5% FS up to 50 MHz, increasing to 5% FS at 100 MHz, Warranted
TRIG (external trigger, V_{pk-pk})	0.25 V up to 100 MHz, increasing to 1 V at 200 MHz, Warranted
Level accuracy	
CH 0, CH 1	±3.5% FS up to 10 MHz
TRIG (external trigger)	±0.35 V (±3.5% of FS) up to 10 MHz
Trigger jitter	≤80 ps _{rms} ²⁵
Trigger filters	
Low-frequency (LF) reject	50 kHz
High-frequency (HF) reject	50 kHz

Digital Trigger

Trigger type	Digital
Sources	PXI_Trig <0..6> (backplane connector) PFI <0..1> (front panel SMB connector)

Video Trigger

Trigger type	Video
Sources	CH 0 (front panel BNC connector) CH 1 (front panel BNC connector) TRIG (front panel BNC connector)

²⁵ Within ±5 °C of self-calibration temperature.

Video trigger types	Specific line Any line Specific field
Standards	Negative sync of NTSC, PAL, or SECAM signal

External Trigger

Connector	TRIG (front panel BNC connector)
Impedance	1 M Ω in parallel with 22 pF
Coupling	AC DC
AC-coupling cutoff (-3 dB)	12 Hz
Input voltage range	± 5 V
Maximum input overload	Peaks ≤ 42 V

Programmable Function Interface (PFI 0 and PFI 1)

Connector	AUX I/O (9-pin mini-circular DIN)
Direction	Bi-directional
As an input (trigger)	
Destinations	Start trigger (acquisition arm) Reference (stop) trigger Arm reference trigger Advance trigger
Input impedance	150 k Ω , nominal
V _{IH}	2.0 V
V _{IL}	0.8 V
Maximum input overload	-0.5 V to 5.5 V
Maximum frequency	25 MHz

As an output (event)

Sources	Ready for Start Start trigger (acquisition arm) Ready for Reference Reference (stop) trigger End of Record Ready for Advance Advance trigger Done (end of acquisition) Probe Compensation ²⁶
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum drive current	± 12 mA
Maximum frequency	25 MHz

Waveform

Table 13. Onboard Memory Size

Memory per Channel	Samples per Channel	Maximum Number of Records in Onboard Memory
8 MB (standard option)	4 MS	16,384
64 MB	32 MS	100,000
256 MB	128 MS	100,000

Minimum record length	1 sample
Number of pretrigger samples	Zero up to full record length ²⁸

²⁶ 1 kHz, 50% duty cycle square wave, PFI 1 only.

²⁷ It is possible to exceed this number if you fetch records while acquiring data.

²⁸ Single-record mode and multiple-record mode.

Number of posttrigger samples	Zero up to full record length ²⁸
Allocated onboard memory per record	(Record Length × 2 bytes/S) + 480 bytes, rounded up to next multiple of 128 bytes or 512 bytes, whichever is greater

Related Information

For more information about fetching records while acquiring data, refer to the [NI High-Speed Digitizers Help](https://ni.com/manuals), available at ni.com/manuals.

Calibration

External Calibration

External calibration calibrates the VCXO and the voltage reference. All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for gain, offset, frequency response, triggering, and timing adjustment errors for all input ranges.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time ²⁹	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE 3.3.1.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-5122. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindowsTM/CVITM

²⁹ Warm-up time begins after the NI-SCOPE driver is loaded. Unless manually disabled, the NI-SCOPE driver automatically loads with the operating system and enables the module.

- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PXIe-5122 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.



Note InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE-specific soft front panel instead of InstrumentStudio.

Interactive control of the PXIe-5122 was first available via InstrumentStudio in NI-SCOPE 2018 and via the NI-SCOPE SFP in NI-SCOPE 2.7. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5122. MAX is included on the driver media.

TClk Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help*, which is located within the *NI High-Speed Digitizers Help*. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

Intermodule SMC Synchronization Using NI-TClk for Identical Modules

Specifications are valid under the following conditions:

- PXI-5122 modules installed in one NI PXI-1042 chassis, or PXIe-5122 modules installed in one PXI Express chassis.
- All parameters set to identical values for each SMC-based module.
- Sample clock set to 100 MS/s and all filters disabled.



Note Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

Skew ³⁰	500 ps
Average skew after manual adjustment ³¹	<10 ps
Sample clock delay/adjustment resolution	≤10 ps

Power

Current draw

+3.3 V DC	1.6 A, maximum
+12 V DC	2.0 A, typical 2.32 A, maximum
Total power	29.28 W, typical 33.12 W, maximum

Dimensions and Weight

Dimensions	3U, one-slot, PXI Express module 21.3 cm × 2.0 cm × 13.0 cm (8.4 in. × 0.8 in. × 5.1 in.)
Weight	453 g (16.0 oz)

³⁰ Caused by clock and analog path delay differences. No manual adjustment performed.

³¹ For information about manual adjustment, refer to the *Synchronization Repeatability Optimization* topic in the *NI-TClk Synchronization Help* available at ni.com/manuals. For additional help with the adjustment process, contact NI Technical Support at ni.com/support.

Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1



Note For UL and other safety certifications, refer to the product label or the [Product Certifications and Declarations](#) section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions

- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.



Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.



Note For EMC declarations, certifications, and additional information, refer to the [Product Certifications and Declarations](#) section.

CE Compliance

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

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