# CPUs, Memory Cards, Memory Submodules, Interface Submodules

# 5

This chapter contains information on the CPUs, memory cards, modules and submodules which you can use in your programmable controller.

The following CPUs may be fitted in an S5-135U/155U central controller:

- CPU 948
- CPU 928B
- CPU 928
- CPU 922.

A programmable controller containing a CPU 948 is known as an S5-155U PLC. A programmable controller containing CPUs 928B, 928 and/or 922 (and not the CPU 948) is known as an S5-135U PLC.

You can fit a flash EPROM memory card containing your user program in the CPU 948, 928B -3UA21 and 928 -3UA21. For the CPUs 928B, 928 and 922, there are RAM or EPROM submodules for the purpose.

CPUs 948 and 928B have, apart from the programmer interface, a second serial interface. An interface submodule is required for physical adaptation.

## Chapter Overview


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## 5.1 CPU 948B -3UA13 or CPU 948B -3UA23

This section contains the hardware description and technical specifications of the CPU 948B -3UA13 or the CPU 948B -3UA23.

Details on programming the CPU 948 can be found in the CPU 948 Programming Guide.

### 5.1.1 Technical Description

This section contains information on the application, design and structure of the CPU 948.

**Application**

You can use the CPU 948 in single and multiprocessor operation in the S5-135U/155U central controller (see Chapter 6).

There are two versions of CPU 948:

- The CPU 948-1 offers 640 Kbytes of internal user memory (RAM).
- The CPU 948-2 offers 1664 Kbytes of internal user memory (RAM).

As an external memory medium, you can use a memory card 374.

The following program processing levels are possible:

- Cyclic
- Time-controlled (9 different timebases, real-time controlled, timeout)
- Interrupt-driven from the S5 bus (8 process interrupts at block boundaries via IB0 or, alternatively, 4 system interrupts)
- Soft STOP.

**Design**

The electronic circuitry of the CPU 948B is on one PCB in the double Eurocard format. The front plate width is 1 1/3 standard plug-in stations, i.e. 20 mm. In the central controller rack, the CPU 948B -3UA13 or the CPU 948B -3UA23 occupies one slot.

## 5.1.2 Installation and Startup

**Jumper Settings**

There are four system interrupts for interrupt-driven program processing with the CPU 948:

- INTA/B/C/D (depending on the CPU slot, see also Section 4.1.1)
- INTE
- INTF
- INTG.

The interrupts you wish to use must be enabled by inserting the jumper plugs provided. The jumper socket is situated on the basic board above the receptacle for the memory card. The exact location is given in Figure 5-1:

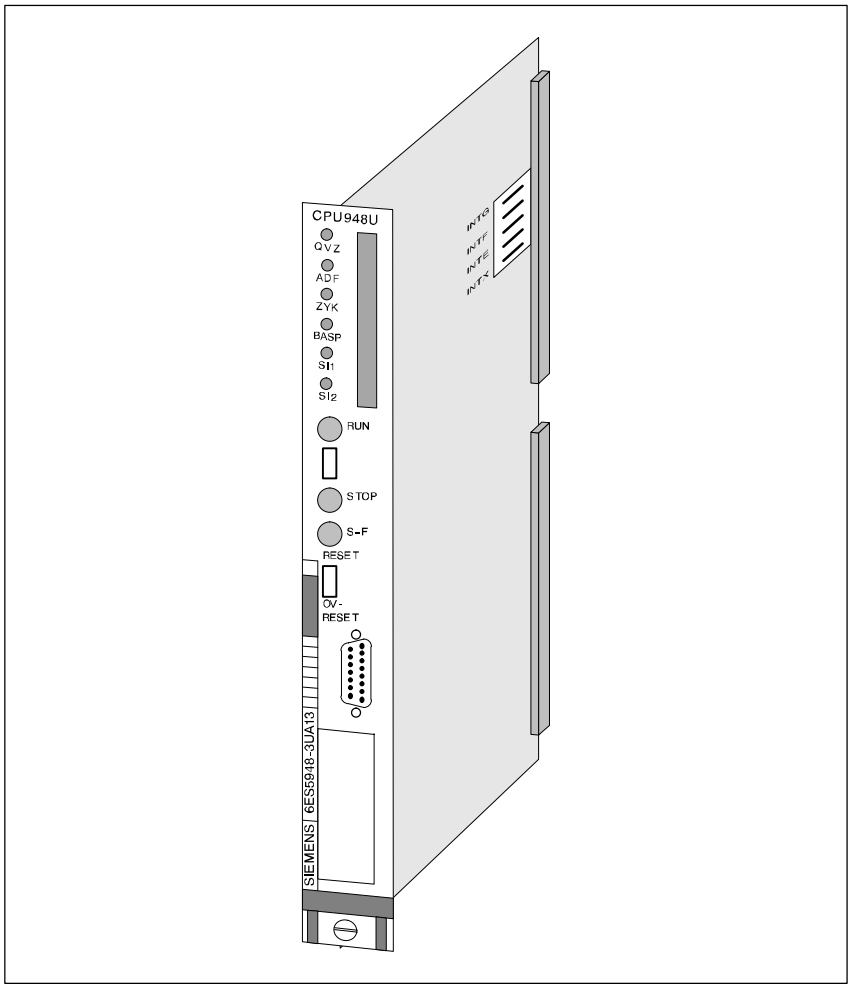



Figure 5-1 Location of Jumper Socket

If you want to operate an IM308C in the IM3/IM4 area and additional digital or analog modules in the central controller, you must insert the jumper shown in Figure 5-1.

**Note**

All other jumpers on the CPU 948B -3UA13 or the CPU 948B -3UA23 are required for quality testing by the manufacturer. You must not change these jumper settings.

## Removing and Inserting the Module



**Caution**

Switch off the power supply before removing or inserting the module.

### Insertion

Proceed as follows to insert the CPU in the central controller:

| Step | Action |
|---|---|
| 1 | Release the upper locking bar of the central controller and ensure that the locking pin for the module is correctly positioned with the slot-head horizontal. |
| 2 | Select the correct slot (based on the labelling of the locking bar). Insert the CPUs in the S5-135U/155U CC from slot 11. |
| 3 | Push the module evenly into the guide rail until the lever over the locking pin is horizontal. |
| 4 | Press the locking pin inwards on the bottom of the module and rotate it 90° clockwise. |
| 5 | Secure the upper locking bar. |

**Note**

If you install the CPU 948 -3UA13 or the CPU 948 -3UA23 as the replacement for a double-width CPU 948, you must cover the slot which has become avaible with a blanking plate.

## Removal

Proceed as follows to remove the CPU:

| Step | Action |
|---|---|
| 1 | Release the upper locking bar of the central controller. |
| 2 | Release the locking pin of the module. |
| 3 | Press the release lever downwards and pull the module forwards and out of the central controller. |

**Note**

Only operate the CPU 948 -3UA13 or the CPU 948 -3UA23 with the submodule receptacle closed. You close it either by fitting an interface submodule or with the cover supplied.

**Controls and Indicators**

The controls and indicators are arranged on the front plate of the CPU module:

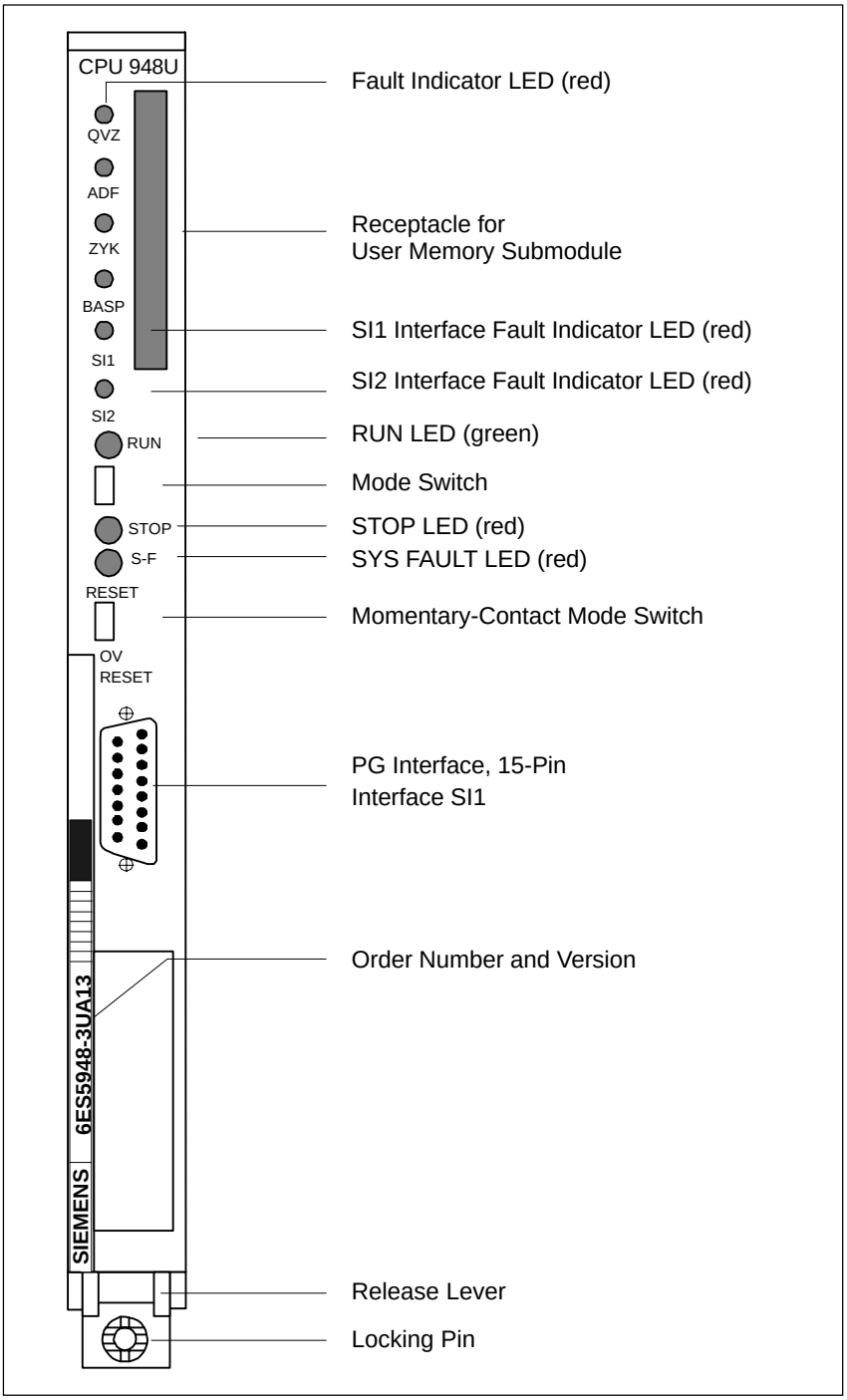



Figure 5-2 Front Plate of the CPU 948-3UA13 or the CPU 948-3UA23

**Mode Switch**

The mode switch has two settings:

**RUN**

In the RUN setting, the CPU 948 processes the user program when the green RUN LED is lit.

**STOP**

The CPU 948 goes to the stop state when you switch from RUN to STOP. The red STOP LED then lights up.

**Momentary-Contact Mode Switch**

You can initiate the Overall Reset, Reset and Restart functions with the momentary-contact mode switch:

**OVERALL RESET**

Momentary-contact switch down
With an overall reset, all RAM areas are erased and initialized (both on the CPU and on a RAM submodule).

**RESET**

Momentary-contact switch up
During a reset, all flags, timers, counters and the process image will be erased. OB 20 will be invoked. Processing of the user program will start from the beginning again.

**Restart**

Momentary-contact switch at midpoint
With a restart, processing of the user program will continue from the point of interruption. The statuses of flags, timers, counters, and the process image are retained during stoppage of the CPU.

## Status Indicators

Given in the following overview are the functions of the RUN, STOP and SYS FAULT status LEDs.

The STOP LED indicates a soft stop; the SYS FAULT LED indicates a hard STOP.

The CPU 948 can process a user program (OB 39) cyclically at the soft STOP, but the digital outputs remain inhibited. At the hard STOP, no program can run and the CPU has “stopped.” This state can only be exited by switching the system voltage off and on again.

| RUN LED | STOP LED | SYS FAULT LED | Status |
|---|---|---|---|
| on | off | off | The CPU is in the RUN state (cyclic operation). |
| on | on | on | Appears briefly after power-up of the unit. |
| off | off | off | CPU is in the initial start or program check state. |
| off | on | off | CPU is in the soft STOP state. |
| off | rapid flashing | off | CPU is in the soft STOP state.<br>Overall reset has been requested by switch or from the operating system. |
| off | slow flashing | off | CPU is in the soft STOP state. An error has occurred; see the CPU 948 Programming Guide for possible causes. |
| off | off | on | CPU is in the hard STOP state. No program processing is taking place. You can only exit from this state by switching the system voltage off and on again. |

## LEDs for Fault Indication and Signaling

Given in the following overview are the causes for LEDs lighting up:

| | |
|---|---|
| **QVZ LED** | |
| on | A module addressed by the program no longer acknowledges although/because<br>• *either* it has acknowledged in single-processor operation upon restart of the CPU 948 in the area of the process image (IB0 to 127, QB0 to 127) and has been entered as present in the so-called 9th track;<br>• *or* it has been entered in multi or single-processor operation in DB 1 (address list) and has been recognized as present during the restart;<br>• *or* it was addressed in direct access by operations LPY, LPW, TPY, TPW, LOY, LOW, TOY, TOW;<br>• *or* the data handling blocks cannot access the module.<br>**Possible causes:**<br>• Module failure<br>• Module removed during operation, in the STOP state or in the Off state without subsequent restart. |
| | A timeout occurred during access to the user memory. |
| **ADF LED** | |
| on | The user program has referred to an address in the process image under which no module was inserted in the I/Os or was not entered in DB 1 during the last restart. |
| **ZYK LED** | |
| on | The preset cycle time monitor has responded and cyclic program processing is interrupted. |
| **BASP LED** | |
| on | Command output is inhibited and the digital outputs will be directly switched to the safe state (0). |

A detailed description of interrupt and error handling can be found in the CPU 948 Programming Guide.

### Fault LEDs SI1 and SI2

LEDs SI1 and SI2 indicate faults in communication via interfaces SI1 and SI2:

| LED SI1 | LED SI2 | Cause |
|---|---|---|
| on | on | Communication is not possible at both interfaces.<br>Internal fault. |
| on | off | SI1:<br>No communication possible.<br>Internal fault.<br><br>SI2:<br>Interface is initialized and ready.<br>LED SI2 is always off if no interface module is inserted. |
| off | on | SI1:<br>Interface is initialized and ready.<br><br>SI2:<br>No communication possible. Wrong module inserted or internal fault. |
| off | off | Both interfaces are initialized and ready.<br><br>LED SI2 is always off if no interface module is inserted. |

### Startup

The module must be inserted at the correct slot in the central controller. The backup battery must be fitted and in order for the CPU to start.

### Overall Reset

Proceed as follows:

| Step | Action | Result |
|---|---|---|
| 1 | Set the mode switch to STOP | |
| 2 | Switch the system voltage on. | The following LEDs must light up on the CPU:<br>– Red STOP LED (flashing rapidly)<br>– Red BASP LED |
| 3 | Hold the operating mode switch in the OVERALL RESET setting and simultaneously set the mode switch from STOP to RUN. | The red STOP LED is now permanently lit. |

If the red SYS FAULT LED also lights up, an error has occurred during overall reset. In this case the measures described must be repeated. If necessary, switch the system voltage off and on again. If the LED is still lit, the module is faulty.

### Reset

Continue as follows:

| Step | Action | Result |
|---|---|---|
| 1 | Set the mode switch to STOP. | |
| 2 | Hold the MC switch in the RESET setting and simultaneously set the mode switch from STOP to RUN. | – Red STOP LED goes off<br>– Green RUN LED lights up<br>– Red BASP LED goes off<br><br>The CPU is now in the RUN state but still has no user program. |

## Restart

You can also carry out a manual restart of the CPU 948 with the mode switch. The CPU 948 Programming Guide will indicate when a manual restart is permissible.

| Step | Action | Result |
|---|---|---|
| 1 | Set the mode switch from STOP to RUN | – Red STOP LED goes off<br>– RUN LED lights up<br>– Red BASP LED goes off |

For maintenance purposes or in the event of a fault, this startup without user program in single-processor operation can serve to establish whether the CPU is operating without errors.

## 5.1.3 Interfaces of the CPU 948

This section contains information on the interfaces of the CPU 948.

**PG Interface SI1**

You can use the PG interface on the CPU 948 either via the front connector or via the 923C coordinator module and the S5 bus.

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**Note**

Simultaneous operation of the PG interface via the front connector of the CPU 948 and via the 923C coordinator is not possible. Switching the PG online without a job request is already sufficient to operate the interface. Electrically, it is merely a PG interface which can be operated via two different terminals.

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The connection to the PG can be established in every operational state of the CPU.

**Second Interface SI2**

You can optionally use the second interface of the CPU 948 -3UA13 or the CPU 948 -3UA23 as:

- A PG interface (for PG and operator panels)
- Interface for the RK 512 computer link
- Interface for data transmission with procedures 3964/3964R
- Interface for data transmission with the “open driver”
- Interface for data transmission via the SINEC L1 bus.

To utilize the second interface as the PG interface, you need the

- PG submodule.

You need one of the following interface submodules for the RK 512 computer link, for data transmission with procedures 3964/3964R and for data transmission with the “open driver”:

- V.24 submodule (RS 232C)
- TTY submodule
- RS422 A/485 submodule (only in the RS422 A module).

To utilize the second interface for data transmission via the SINEC L1 bus, you need the

- SINEC L1 submodule.

The CPU 948 -3UA13 or the CPU 948 -3UA23 is delivered without an interface submodule. You can operate the CPU 948 -3UA13 or the CPU 948 -3UA23 without an integral interface submodule. The opening to accept a submodule in the front plate is closed by a cover. Only remove the cover to fit an interface submodule.

A description of interface submodules can be found in Section 5.11, and the order numbers in the ordering information.

A detailed description of the second interface can be found in the CPU 928B/CPU 948 Communication Manual.

### Communication via Backplane Bus with SINEC H1

A PG-PLC link via SINEC H1 allows very advanced communication between the partners. For example, the user software can be loaded into the CPU 948 up to eight-times faster than with serial communication.

For this link you will need, in addition to the CPU 948, a CPU 143 (Version $\geq$ 2.1) in the PLC and a PG7xx with SINEC H1 connection and the STEP 5 single-tasking software from Version 6.0 or multi-tasking from Version 2.0.

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**Note**

You cannot implement communication via SINEC H1 in parallel with the serial interfaces.

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Communication via SINEC H1 is described in detail in the CPU 948 Programming Guide.

## 5.1.4 Technical Specifications

**Important for the USA and Canada**

The following approvals have been obtained:

- UL Listing Mark
  Underwriters Laboratories (UL) to Standard UL 508, Report E 85972
- CSA Certification Mark
  Canadian Standard Association (CSA) to Standard C 22.2 No. 142, Report LR 63533

| | | | | | |
|---|---|---|---|---|---|
| Degree of protection | IP 00 | | | | |
| Climatic ambient conditions | See Technical Specifications of the S5-135U/155U CC | | | | |
| Mechanical ambient conditions | See Technical Specifications of the S5-135U/155U CC | | | | |
| Noise immunity, electromagnetic compatibility (EMC) | See Technical Specifications of the S5-135U/155U CC | | | | |
| Supply voltage | 5 V ± 5 %<br>24 V + 25 %/ –17 % | | | | |
| Current consumption at 5 V | 1.5 A typical | | | | |
| Backup voltage | 3.4 V | | | | |
| Backup current | 20 µA typical (at 25 °C) | | | | |
| | P area | O area | IM3 area | IM4 area | Total |
| Digital inputs with process image<br>Digital inputs without process image<br>or analog inputs | 1024 max.<br>1024 max.<br>64 max. | –<br>2048 max.<br>128 max. | –<br>2048 max.<br>128 max. | –<br>2048 max.<br>128 max. | 1024 max.<br>7168 max.<br>448 max. |
| Digital outputs with process image<br>Digital outputs without process image<br>or analog outputs | 1024 max.<br>1024 max.<br>64 max. | –<br>2048 max.<br>128 max. | –<br>2048 max.<br>128 max. | –<br>2048 max.<br>128 max. | 1024 max.<br>7168 max.<br>448 max. |
| Flags | 2048 | | | | |
| S flags | 32768 | | | | |
| Timers | 256 | | | | |
| Counters | 256 | | | | |
| Size of user memory | 64 x $2^{10}$ bytes max., RAM | | | | |
| Transmission rate of the serial PG interface | 9600 bps | | | | |
| Program blocks PB | 256 | | | | |
| Sequence blocks SB | 256 | | | | |
| Function blocks FB | 256 | | | | |
| Function blocks FX | 256 | | | | |

| | |
|---|---|
| Data blocks DB | 256, of which 253 are freely available |
| Data blocks DX | 256, of which 253 are freely available |
| Organization blocks OB | OB 1 to 39 (interfaces for operating system) |
| Integrated special function organization blocks OB | OB 121, 122, 124-126, 131-133, 141-143, 150, 151, 153, 200, 202-205, 222, 223, 254, 255 |
| Integrated serial interface | PG interface |
| Optional serial interface | Via interface submodules, optionally as V.24, TTY, RS422 A/485 submodule, SINEC L1 or PG interface |
| Backplane bus | S5 bus |
| Dimensions (w x h x d) | 20.32 x 233.4 x 160 mm |
| Weight | Approx. 0.6 kg |

## For Chapter 5

| | |
|---|---|
| **CPUs** | |
| CPU 948-1 (640 Kbyte user memory)<br>CPU 948-2 (1664 Kbyte user memory) | 6ES5 948-3UA13<br>6ES5 948-3UA23 |
| CPU 928B | 6ES5 928-3UB21 |
| CPU 928 | 6ES5 928-3UA21 |
| CPU 922 | 6ES5 922-3UA11 |
| **374 Memory Cards** | |
| 256 Bbytes<br>512 Bbytes<br>1028 Bbytes<br>2048 Bbytes<br>4112 Bbytes | 6ES5 374-2FH21<br>6ES5 374-2FJ21<br>6ES5 374-2FK21<br>6ES5 374-2FL21<br>6ES5 374-2FM21 |
| **376 Memory Cards** | |
| 16 Bbytes<br>32 Bbytes<br>64 Bbytes | 6ES5 376-0AA11<br>6ES5 376-0AA21<br>6ES5 376-0AA31 |
| **377 Memory Cards** | |
| 16 Bbytes<br>32 Bbytes<br>64 Bbytes<br>64 Kbytes (with backup battery)<br>Backup battery | 6ES5 377-0AA11<br>6ES5 377-0AA21<br>6ES5 377-0AA32<br>6ES5 377-0BA31<br>6ES5 980-0DA11 |
| **Interface Submodules** | |
| PG submodule<br>TTY submodule for 20 mA current loop<br>V.24 (RS-232C) submodule<br>RS422-A/485 submodule<br>SINEC L1 submodule | 6ES5 752-0AA53<br>6ES5 752-0AA12<br>6ES5 752-0AA22<br>6ES5 752-0AA42<br>6ES5 752-0AA62 |
| Cover for submodule receptacle | C79458-L957-B51 |
| BT 777 bus terminal | 6ES5 777-xxx00 |
| Standard connecting cables<br>CPU 948/928B - PG 7xx<br>CPU 928B - CP 544/525/524 (RS422-A/485)<br>CPU 928B - CP 544/525/524 (TTY)<br>CPU 928B - CP 544/525/524 (V.24)<br>CPU 928B - DR 210/DR 211 DR 230/DR 231 (TTY/V.24) | <br>6ES5 734-2xxx0<br><br>6ES5 725-7xxx0<br>6ES5 726-1xxx0<br>6ES5 726-8xxx0<br><br>6ES5 726-5xxx0 |
| (xxx = SIMATIC length code, see Catalog) | |