

# Schematics Only for RK3576 EVB1

## RK\_EVB1\_RK3576\_LP4XD200P132SD6\_V12

### Main Functions Introduction

- 1) PMIC: 1 x RK806S-5 + DiscretePower
- 2) RAM: 1 x LPDDR4X 32bit(Option 1 x LPDDR4 32bit)
- 3) ROM: 1 x eMMC5.1 + 1 x UFS2.0 (Option SPI Nand Falsh)
- 4) Support: 1 x Micro SD Card3.0
- 5) Support: 1 x USB TYPEC + 1 x USB3.2 Gen1x1 HOST1
- 6) Support: 1 x PCIe Slot (Option)
- 7) Support: 1 x 4Lanes MIPI DCPHY RX Camera(Need Ext Board)
- 8) Support: 2 x 4Lanes or 4 x 2Lanes MIPI DPHY RX Camera(Need Ext Board)
- 9) Support: 1 x 4Lanes MIPI DSI TX with Touch Connector
- 10) Support: 1 x HDMI2.1 TX (Up to 4Kx2K@120Hz)
- 11) Support: 1 x a/b/g/n/ac/ax 2T2R PCIe WIFI6 + UART/PCM BT
- 12) Support: 2 x 10/100/1000M Ethernet
- 13) Support: 1 x Headphone + 2 x SPK + 1 x Analog MIC
- 14) Support: 1 x Array MIC Connector(Ext PDM MicArray Board)
- 15) Support: 1 x IR Receiver
- 16) Support: 1 x G-Sensor
- 17) Support: Array Key(MENU,VOL+,VOL-,ESC)
- 18) Support: 7 x SARADC + 1 x SARADC only for boot
- 19) Support: 1 x Debug UART to USB connector and 1 x JTAG Connector
- 20) Support: 1 x CAN(Option)
- 21) Support: 3 x LED

### Note:

The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic. If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

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Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	00.Cover Page		
Date:	Wednesday, April 01, 2026	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 1 of 49

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## Generate Bill of Materials

### Header:

Item\Part\Description\PCB Footprint\Reference\Quantity\Option

### Combined property string:

{Item}\{Value}\{Description}\{PCB Footprint}\{Reference}\{Quantity}\{Option}

Description

Note

Option

## Notes

### NOTE 1:

#### Component parameter description

1. NC stands for component not mounted temporarily
2. If Value or option is NC, which means the area is reserved without being mounted

### NOTE 2:

Please use our recommended components to avoid too many changes.  
For more informations about the second source,please refer to our AVL.

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Project: RK\_EVB1\_RK3576\_LP4XD200P132SD6

File: 01.Index and Notes


Date: Wednesday, April 01, 2026 Rev: V1.2

Designed by: Wesley Huang Reviewed by: Sheet: 2 of 49

# Revision History

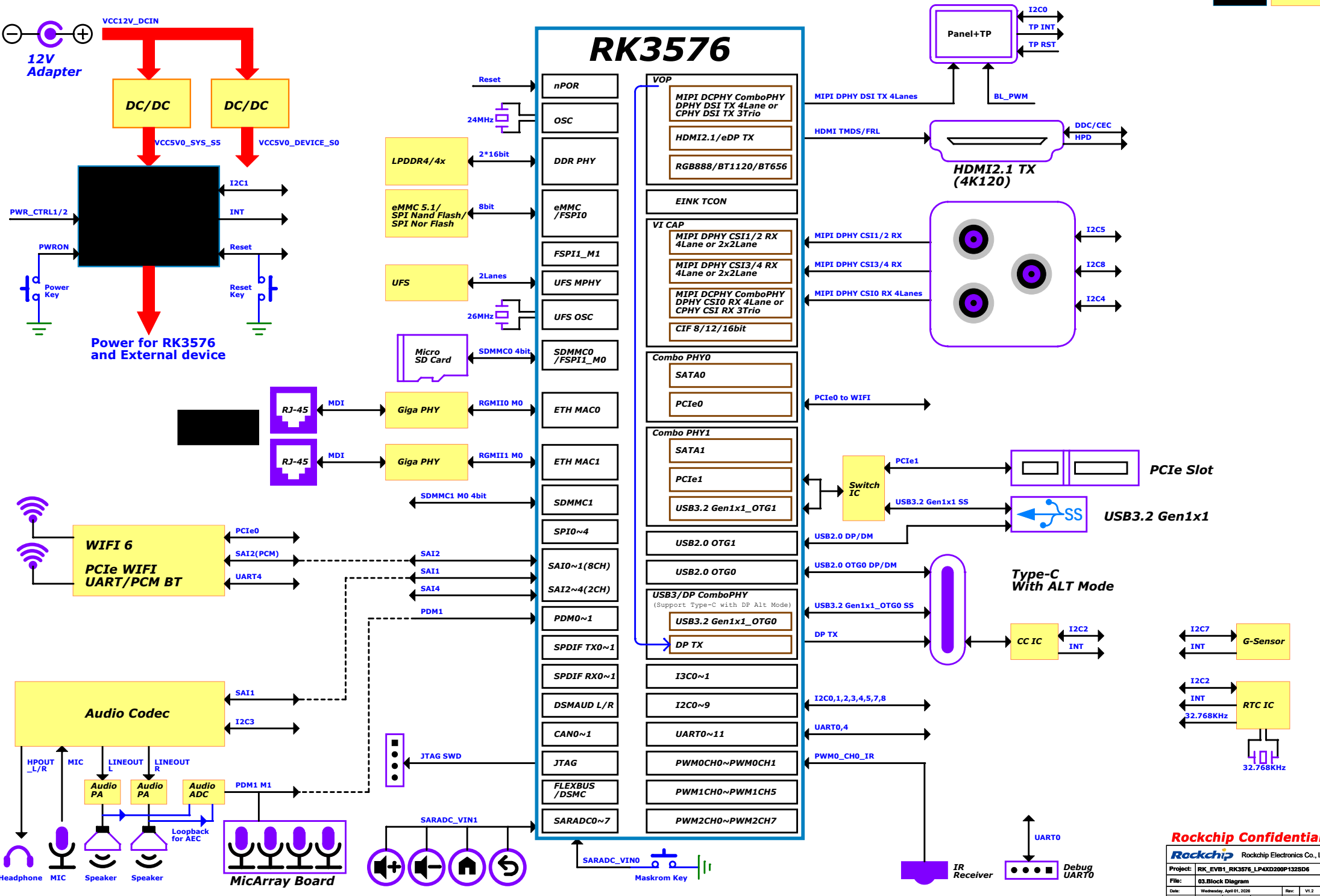
Version	Date	By	Change Description	Approved
V3.0	2026-4-01	Tom	1: USB3.0 differential lines optimization 2: add TWO GND LAYERS and FB OPTIMIZATION	

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<b>Project:</b>	RK_EVB1_RK3576_LP4XD200P132SD6		
<b>File:</b>	02.Revision History		
<b>Date:</b>	Wednesday, April 01, 2026	<b>Rev:</b>	V1.2
<b>Designed by:</b>	Wesley Huang	<b>Reviewed by:</b>	
		<b>Sheet:</b>	3 of 49

# RK3576 Ref Block Diagram (Typical Application Case)

Other IC



# Power Tree

12V/3A Adapter

VCC12V\_DCIN

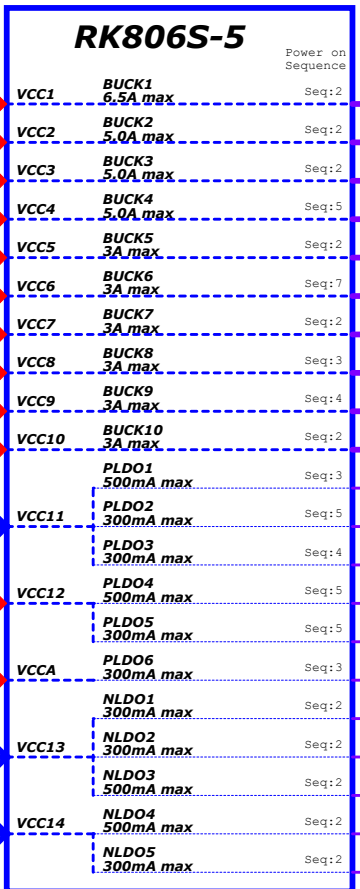
DC/DC 5000mA

DC/DC 3000mA

**Note:**  
With PCIe, the current is estimated according to the actual number of PCIe

VCC5V0\_SYS\_S5  
Seq:0

VCC5V0\_DEVICE\_S0  
Seq:5A



- LDO, 0.5A
- VBUS5V0\_TYPEC
- VCC5V0\_USB3\_HOST
- MIPI CSI RX0/1/2/3/4\_CON\_5V
- MIPI DSI TX\_LCD\_5V
- SPK\_AMP\_5V
- MicArray\_CON\_5V
- TCAN1044V-Q1\_CAN\_3V3
- VCC5V\_HDMI\_TX
- Breathing LED & Work LED

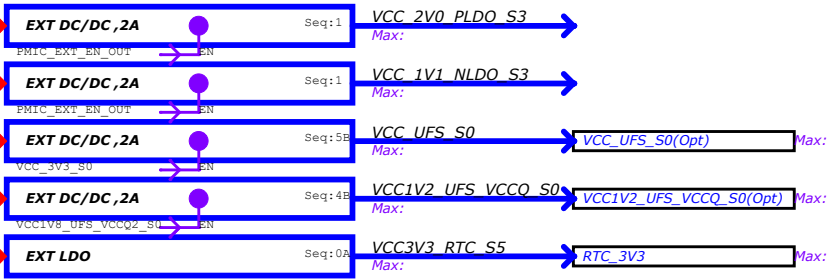
- Power LED
- MIPI CSI RX0/1/2/3/4\_CON\_12V
- FAN
- WIFI/BT-Ext Board
- PCIe1\_Slot\_3V3
- PCIe1\_Slot\_12V
- VCC3V3\_CLK(3V3,PCIe Clock IC)

**Note:**  
The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic. If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

VCC 2V0\_PLDO S3

VCC 1V1\_NLDO S3

VCC 1V1\_NLDO S3



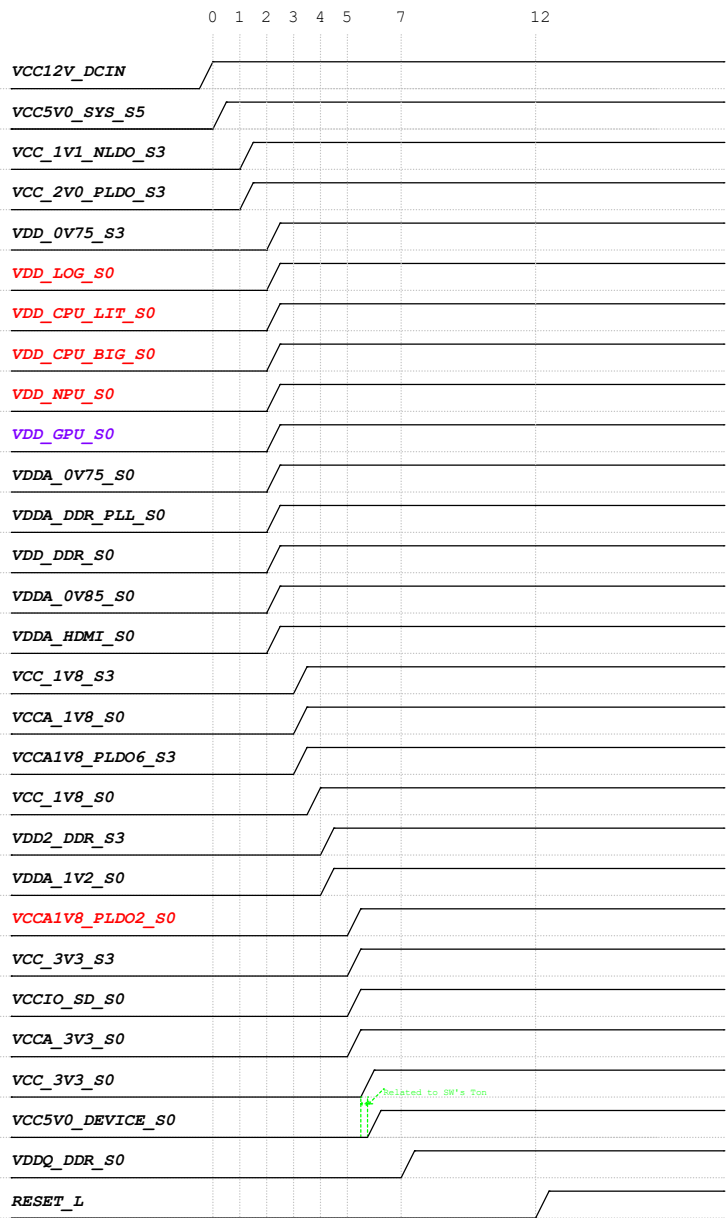
- VDD\_CPU\_BIG\_S0
- VDD\_NPU\_S0
- VDD\_CPU\_LIT\_S0
- VCC\_3V3\_S3
- VDD\_GPU\_SOC
- VDDQ\_DDR\_S0
- VDD\_LOGIC\_S0
- VCC\_1V8\_S3
- VDD2\_DDR\_S3
- VDD\_DDR\_S0
- VCCA\_1V8\_S0
- VCCA\_1V8\_PLDO2\_S0
- VDDA\_1V2\_S0
- VCCA\_3V3\_S0
- VCCIO\_SD\_S0
- VCCA1V8\_PLDO6\_S3
- VDD\_0V75\_S3
- VDDA\_DDR\_PLL\_S0
- VDDA0V75\_HDMI\_S0
- VDDA\_0V85\_S0
- VDDA\_0V75\_S0
- VCC\_2V0\_PLDO\_S3
- VCC\_1V1\_NLDO\_S3
- VCC\_UFS\_S0
- VCC1V2\_UFS\_VCCQ\_S0
- VCC3V3\_RTC\_S5

- LOAD SWITCH VCC\_3V3\_S0
- PMOS
- LOAD SWITCH
- HUSB311\_CC\_3V3
- IR\_3V3
- FT232RL\_3V3
- PCIe WIFI-AP6276P
- WIFI/BT-Ext Board
- PMUIO1\_VCC\_SOC
- LOAD SWITCH VCC\_1V8\_S0
- PMOS
- LPDDR4/4X\_VDD1
- WIFI/BT-Ext Board
- PCIe WIFI-AP6276P
- PMUIO0\_VCC1V8\_SOC
- VCCIO3\_VCC\_SOC
- OSC\_AVDD1V8\_SOC
- PLL\_AVDD1V8\_SOC
- DDRPHY\_PLL\_AVDD1V8\_SOC
- UFS\_AVDD1V8\_SOC
- USB3\_OTG0/DP\_TX\_AVDD1V8\_SOC
- USB2\_OTG\_AVDD1V8\_SOC
- MIPI\_D/C\_PHY\_AVDD1V8\_SOC
- MIPI\_CSI1/2\_AVDD1V8\_SOC
- MIPI\_CSI3/4\_AVDD1V8\_SOC
- HDMI\_TX/eDP\_TX\_AVDDIO1V8\_SOC
- HDMI\_TX/eDP\_TX\_AVDDCMN1V8\_SOC
- PCIe0\_SATA0\_AVDD1V8\_SOC
- PCIe1\_SATA1\_USB3\_OTG1\_AVDD1V8\_SOC
- OSC\_UFS\_AVDD\_SOC
- UFS\_AVDD0V85\_SOC
- USB3\_OTG0/DP\_TX\_AVDD0V85\_SOC
- USB3\_OTG0/DP\_TX\_DVDD0V85\_SOC
- PCIe0\_SATA0\_AVDD0V85\_SOC
- PCIe1\_SATA1\_USB3\_OTG1\_AVDD0V85\_SOC
- PLL\_DVDD0V75\_SOC
- OTP\_DVDD0V75\_SOC
- USB2\_OTG\_DVDD0V75\_SOC
- MIPI\_DCPHY\_AVDD\_SOC
- MIPI\_CSI1/2\_RX\_AVDD0V75\_SOC
- MIPI\_CSI3/4\_RX\_AVDD0V75\_SOC
- VCC\_UFS\_S0(Opt)
- VCC1V2\_UFS\_VCCQ\_S0(Opt)
- RTC\_3V3
- eMMC\_3V3
- VCC\_UFS\_S0
- MIPI CSI RX0/1/2/3/4\_CON\_3V3
- RGMIIL\_PHY0/1\_3V3
- SW\_3V3(FSUSB30MUX/GMA340)
- G-SENSOR\_3V3
- VCCIO4\_VCC\_SOC
- VCCIO6\_VCC\_SOC
- USB2\_OTG\_AVDD3V3\_SOC
- VCC3V3\_LCD\_S0
- VCC3V3\_SD\_S0
- eMMC\_1V8
- FSPI\_1V8
- ES8388/ES7202\_AUDIO\_1V8
- MIPI CSI RX0/1/2/3/4\_CON\_1V8
- VCCIO0\_VCC1V8\_SOC
- VCCIO2\_VCC\_SOC
- VCCIO5\_VCC\_SOC
- UFS\_VCCQ2\_1V8\_S0

**Note:**  
Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

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# Power Sequence



# Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETh								
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

## Note:

The power suffix S0, S3 or S5 means:  
 S5: Keep power on during power down  
 S3: Keep power on during sleeping  
 S0: Power off during sleeping

## Note:

Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

# IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

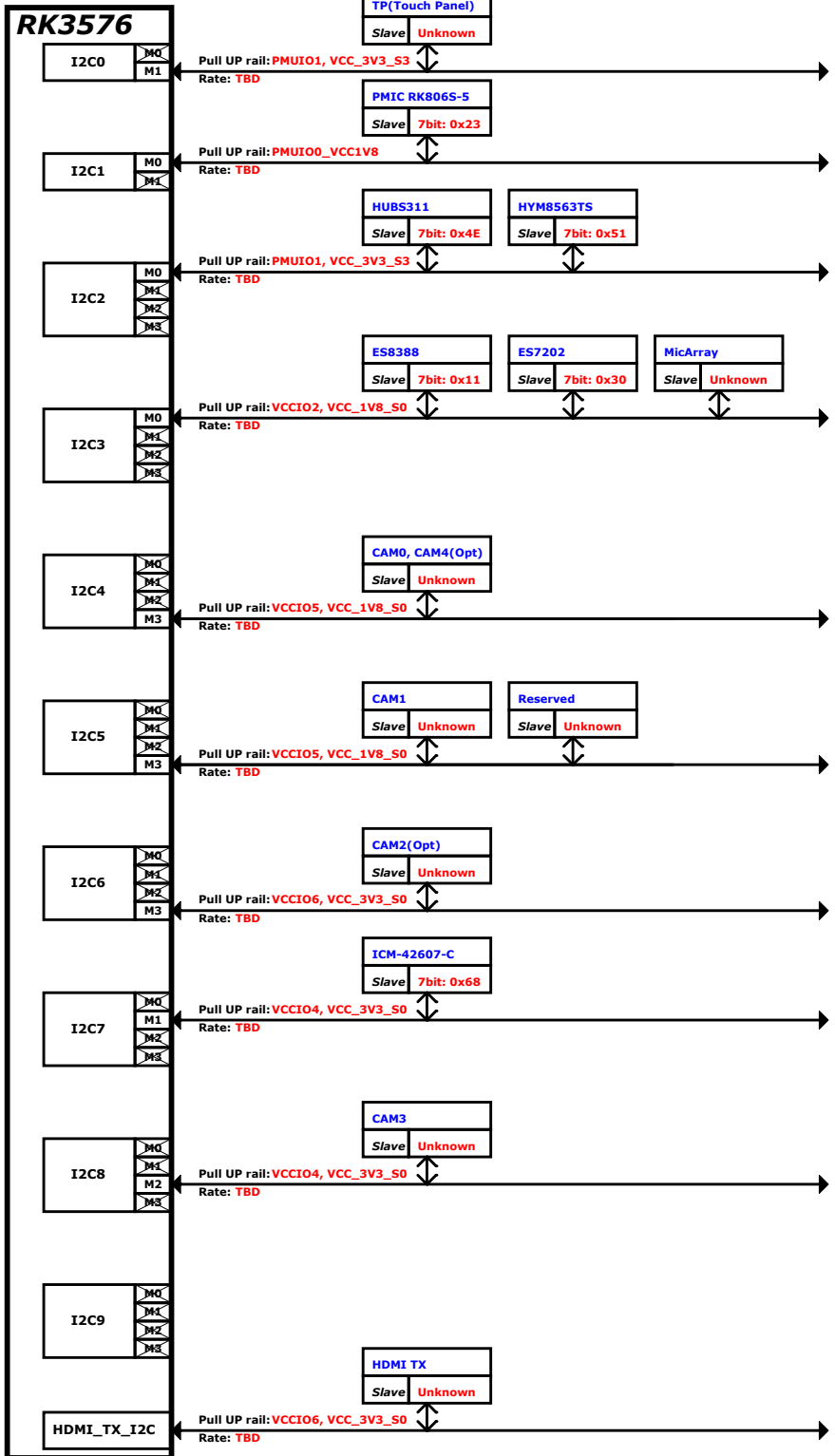
IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

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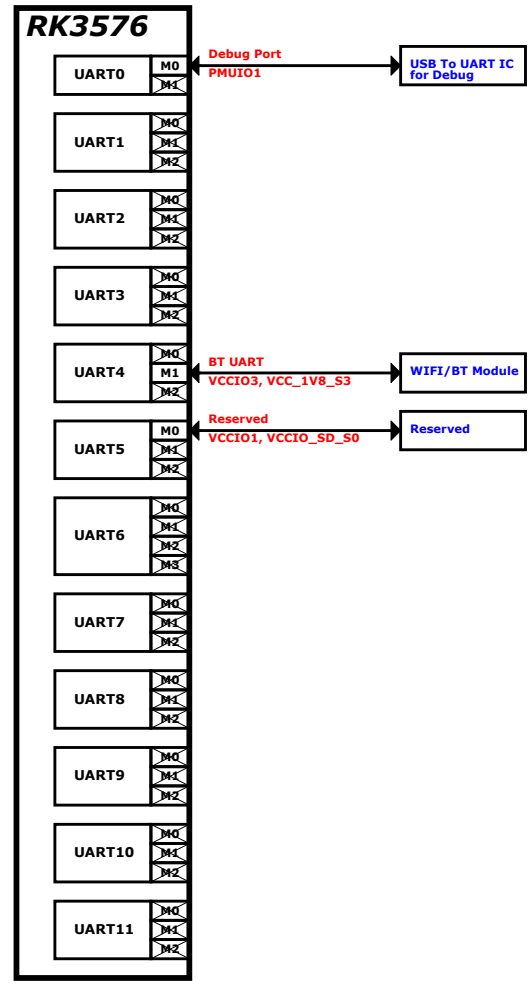
**Rockchip** Rockchip Electronics Co., Ltd

Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	05.Power Sequence and Map		
Date:	Wednesday, April 01, 2026	Rev:	V1.2
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Sheet:	6	of	49

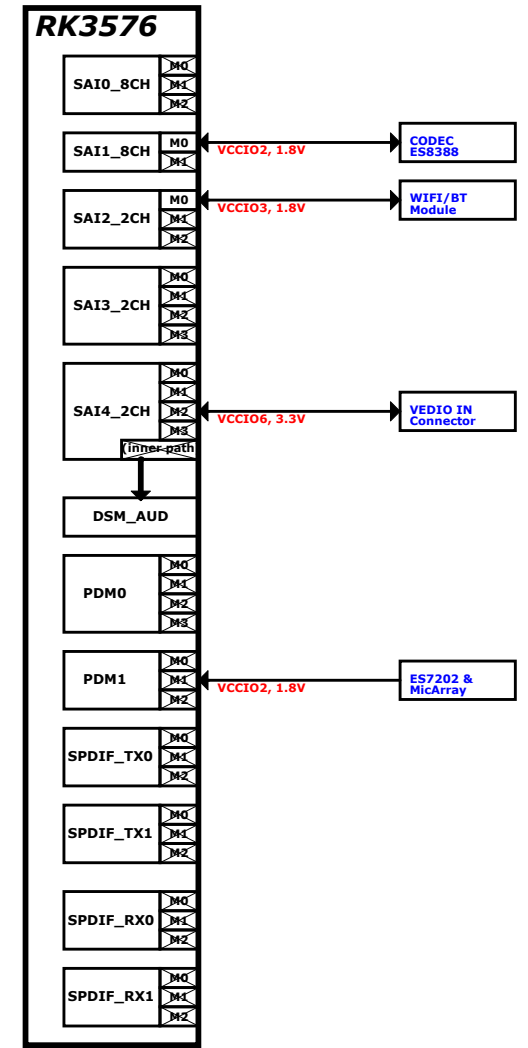
# I2C MAP



# UART MAP



# Audio MAP



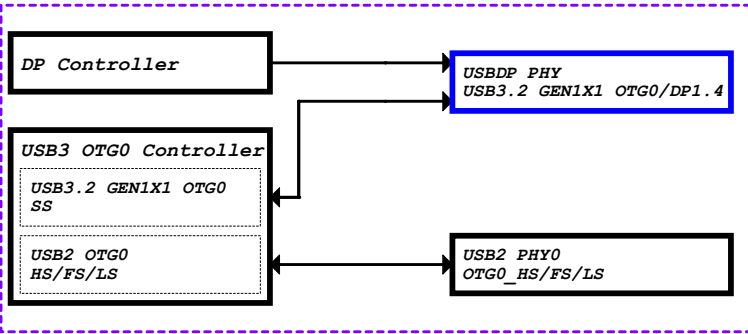
**Note:**

- Unselected IOMUX path
- IOMUX path in use

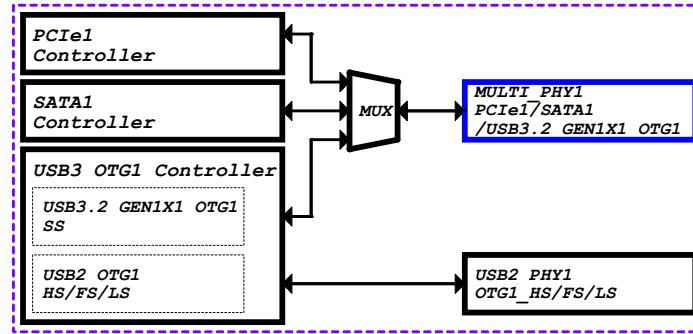
At the same time, only one path can be selected.

# MULTI\_PHY Path Map

## USBDP PHY--USB3.2 GEN1X1 OTG0/DP1.4



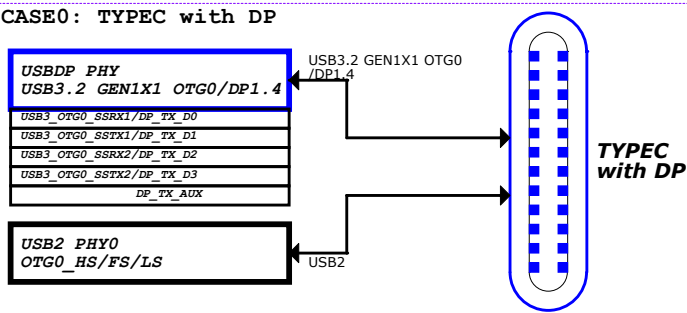
## PCIe Combo PHY1-- PCIe1/SATA1/USB3.2 GEN1X1 OTG1



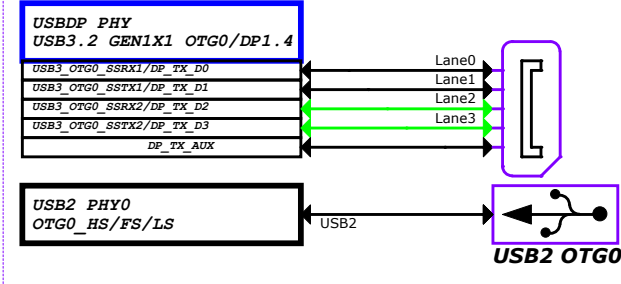
**Note:**  
USB2 PHY1 can only be used when  
PCIe1/SATA1 is not in use!!!

# USB OTG0/DP Application

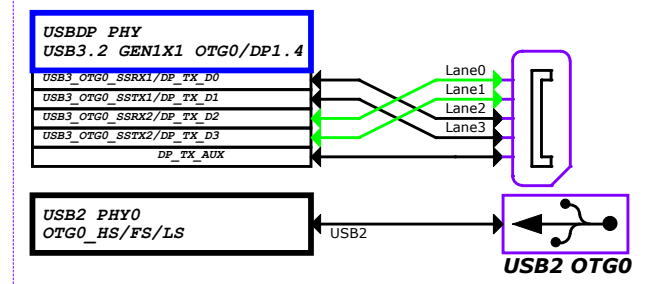
### CASE0: TYPEC with DP



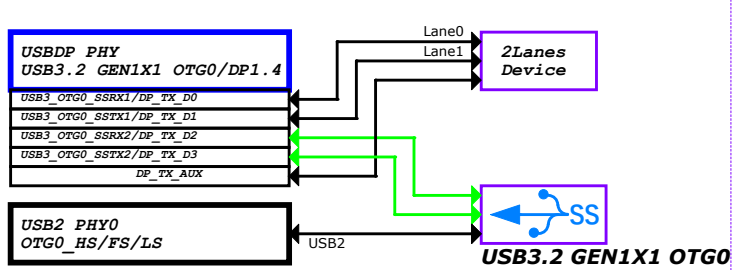
### CASE1: USB2 OTG0 + DP 4Lane (Swap OFF)



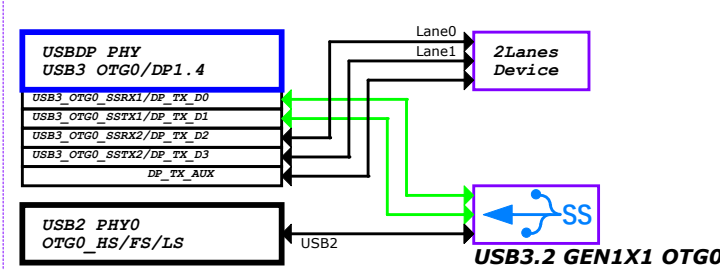
### CASE2: USB2 OTG0 + DP 4Lane (Swap ON)



### CASE3: USB3.2 GEN1X1 OTG0 + DP 2Lane (Swap OFF)



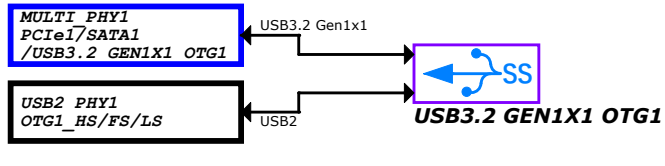
### CASE4: USB3.2 GEN1X1 OTG0 + DP 2Lane (Swap ON)



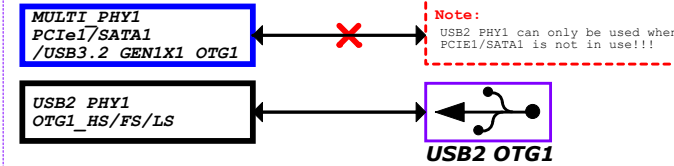
**Note:**  
DP Lane swap enable  
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3\_TXDP/N  
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1\_TXDP/N

# USB OTG1 Application

### CASE0: USB3.2 GEN1X1 OTG1

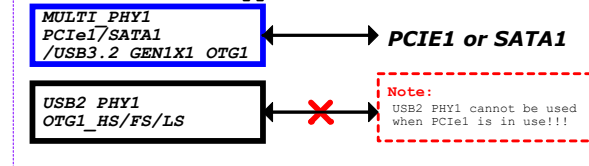


### CASE1: USB2 OTG1



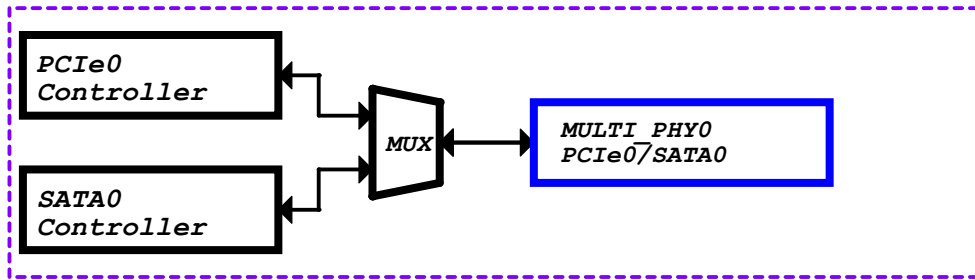
**Note:**  
USB2 PHY1 can only be used when  
PCIe1/SATA1 is not in use!!!

### CASE2: Do not support USB

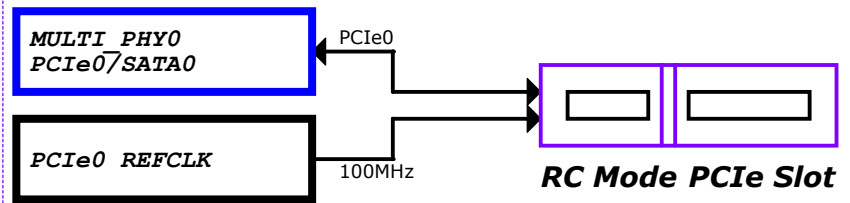


**Note:**  
USB2 PHY1 cannot be used  
when PCIe1 is in use!!!

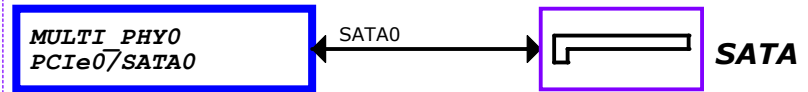
## PCIe Combo PHY0--PCIe0/SATA0



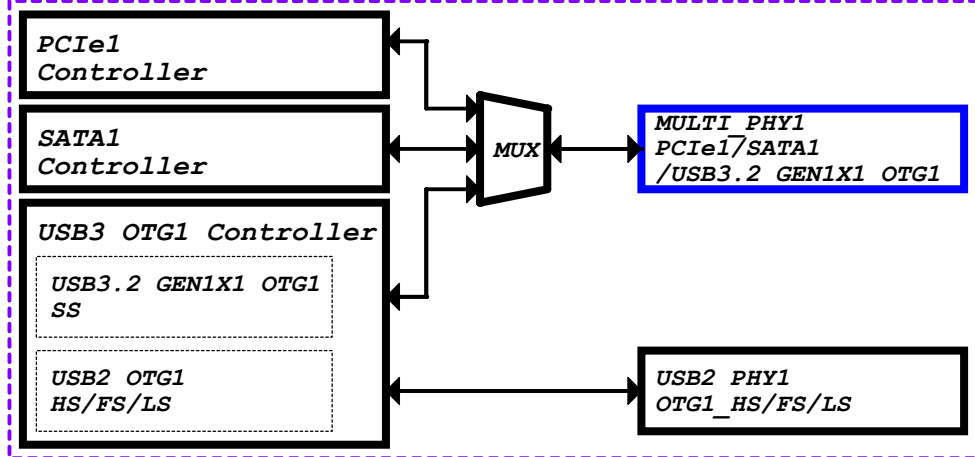
### CASE0: PCIe x 1Lane



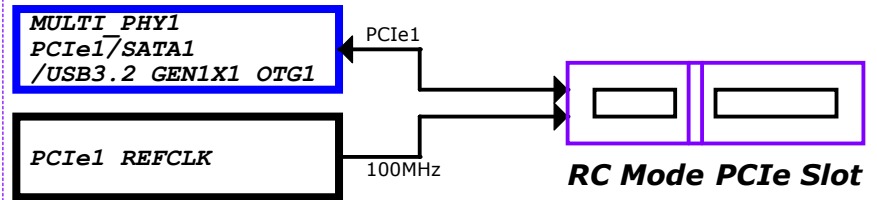
### CASE1: SATA



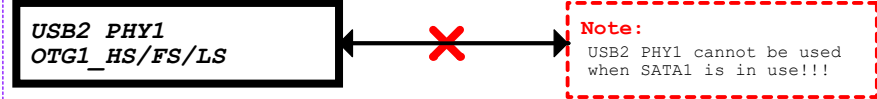
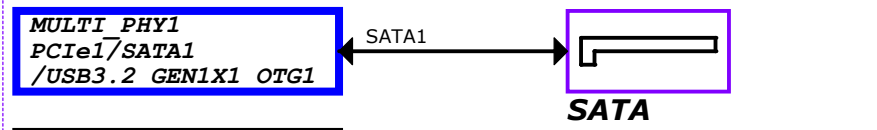
## PCIe Combo PHY1--PCIe1/SATA1/USB3.2 GEN1X1 OTG1



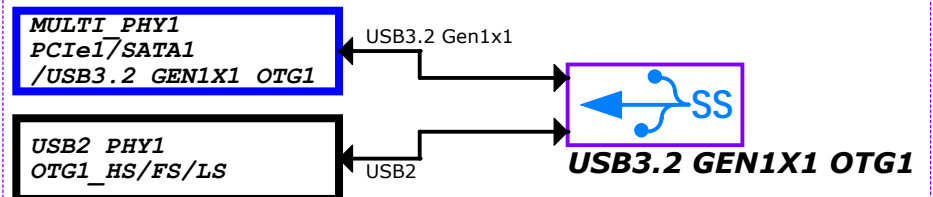
### CASE0: PCIe x 1Lane



### CASE1: SATA



### CASE2: USB3.2 GEN1X1 OTG1



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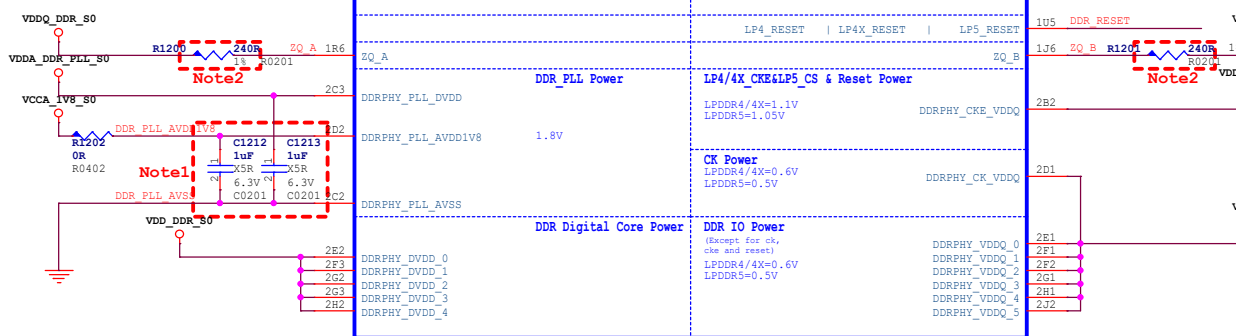
Rockchip		Rockchip Electronics Co., Ltd	
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	08.PCIe Combo PHY Configure Map		
Date:	Wednesday, April 01, 2026	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	
		Sheet:	9 of 49





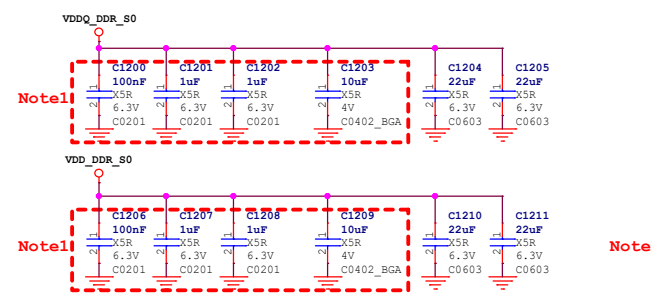
# RK3576\_A (DDRPHY)

U1000A							
	LPDDR4	LPDDR4X	LPDDR5	LPDDR4	LPDDR4X	LPDDR5	
DDR DQ0 A	W1	LP4_DQ0_A	LP4X_DQ0_A	LP5_DQ0_A	LP4_DQ0_B	LP4X_DQ0_B	LP5_DQ0_B
DDR DQ1 A	1P1	LP4_DQ1_A	LP4X_DQ1_A	LP5_DQ1_A	LP4_DQ1_B	LP4X_DQ1_B	LP5_DQ1_B
DDR DQ2 A	1P1	LP4_DQ2_A	LP4X_DQ2_A	LP5_DQ2_A	LP4_DQ2_B	LP4X_DQ2_B	LP5_DQ2_B
DDR DQ3 A	U1	LP4_DQ3_A	LP4X_DQ3_A	LP5_DQ3_A	LP4_DQ3_B	LP4X_DQ3_B	LP5_DQ3_B
DDR DQ4 A	1V3	LP4_DQ4_A	LP4X_DQ4_A	LP5_DQ4_A	LP4_DQ4_B	LP4X_DQ4_B	LP5_DQ4_B
DDR DQ5 A	1W4	LP4_DQ5_A	LP4X_DQ5_A	LP5_DQ5_A	LP4_DQ5_B	LP4X_DQ5_B	LP5_DQ5_B
DDR DQ6 A	AC1	LP4_DQ6_A	LP4X_DQ6_A	LP5_DQ6_A	LP4_DQ6_B	LP4X_DQ6_B	LP5_DQ6_B
DDR DQ7 A	AB1	LP4_DQ7_A	LP4X_DQ7_A	LP5_DQ7_A	LP4_DQ7_B	LP4X_DQ7_B	LP5_DQ7_B
DDR DM0 A	1V1	LP4_DM10_A	LP4X_DM10_A	LP5_DM10_A	LP4_DM10_B	LP4X_DM10_B	LP5_DM10_B
DDR DQS0P A	1U1	LP4_DQS0P_A	LP4X_DQS0P_A	LP5_RDQS0P_A	LP4_DQS0P_B	LP4X_DQS0P_B	LP5_RDQS0P_B
DDR DQSUN A	Y1	LP4_DQSUN_A	LP4X_DQSUN_A	LP5_RDQSUN_A	LP4_DQSUN_B	LP4X_DQSUN_B	LP5_RDQSUN_B
	1V5	--	--	LP5_WCK0P_A	--	--	LP5_WCK0P_B
	1V4	--	--	LP5_WCK0N_A	--	--	LP5_WCK0N_B
DDR DQ8 A	AF1	LP4_DQ8_A	LP4X_DQ8_A	LP5_DQ8_A	LP4_DQ8_B	LP4X_DQ8_B	LP5_DQ8_B
DDR DQ9 A	1AB1	LP4_DQ9_A	LP4X_DQ9_A	LP5_DQ9_A	LP4_DQ9_B	LP4X_DQ9_B	LP5_DQ9_B
DDR DQ10 A	1AD1	LP4_DQ10_A	LP4X_DQ10_A	LP5_DQ10_A	LP4_DQ10_B	LP4X_DQ10_B	LP5_DQ10_B
DDR DQ11 A	AH1	LP4_DQ11_A	LP4X_DQ11_A	LP5_DQ11_A	LP4_DQ11_B	LP4X_DQ11_B	LP5_DQ11_B
DDR DQ12 A	1Y1	LP4_DQ12_A	LP4X_DQ12_A	LP5_DQ12_A	LP4_DQ12_B	LP4X_DQ12_B	LP5_DQ12_B
DDR DQ13 A	1W2	LP4_DQ13_A	LP4X_DQ13_A	LP5_DQ13_A	LP4_DQ13_B	LP4X_DQ13_B	LP5_DQ13_B
DDR DQ14 A	1AA3	LP4_DQ14_A	LP4X_DQ14_A	LP5_DQ14_A	LP4_DQ14_B	LP4X_DQ14_B	LP5_DQ14_B
DDR DQ15 A	1AA1	LP4_DQ15_A	LP4X_DQ15_A	LP5_DQ15_A	LP4_DQ15_B	LP4X_DQ15_B	LP5_DQ15_B
DDR DM1 A	AE1	LP4_DM11_A	LP4X_DM11_A	LP5_DM11_A	LP4_DM11_B	LP4X_DM11_B	LP5_DM11_B
DDR DQS1P A	1AB4	LP4_DQS1P_A	LP4X_DQS1P_A	LP5_RDQS1P_A	LP4_DQS1P_B	LP4X_DQS1P_B	LP5_RDQS1P_B
DDR DQSIN A	1AB3	LP4_DQSIN_A	LP4X_DQSIN_A	LP5_RDQSIN_A	LP4_DQSIN_B	LP4X_DQSIN_B	LP5_RDQSIN_B
	1AA6	--	--	LP5_WCK1P_A	--	--	LP5_WCK1P_B
	1AA5	--	--	LP5_WCK1N_A	--	--	LP5_WCK1N_B
DDR A0 A	T1	LP4_A0_A	LP4X_A0_A	LP5_A0_A	LP4_A0_B	LP4X_A0_B	LP5_A0_B
DDR A1 A	1N1	LP4_A1_A	LP4X_A1_A	LP5_A1_A	LP4_A1_B	LP4X_A1_B	LP5_A1_B
DDR A2 A	1R3	LP4_A2_A	LP4X_A2_A	LP5_A2_A	LP4_A2_B	LP4X_A2_B	LP5_A2_B
DDR A3 A	1T2	LP4_A3_A	LP4X_A3_A	LP5_A3_A	LP4_A3_B	LP4X_A3_B	LP5_A3_B
DDR A4 A	1M5	LP4_A4_A	LP4X_A4_A	LP5_A4_A	LP4_A4_B	LP4X_A4_B	LP5_A4_B
DDR A5 A	1P5	LP4_A5_A	LP4X_A5_A	LP5_A5_A	LP4_A5_B	LP4X_A5_B	LP5_A5_B
	1R5	--	--	LP5_A6_A	--	--	LP5_A6_B
DDR CLKP A	1L1	LP4_CLKP_A	LP4X_CLKP_A	LP5_CLKP_A	LP4_CLKP_B	LP4X_CLKP_B	LP5_CLKP_B
DDR CLKN A	P1	LP4_CLKN_A	LP4X_CLKN_A	LP5_CLKN_A	LP4_CLKN_B	LP4X_CLKN_B	LP5_CLKN_B
LPDDR4 CSN0 A	1R4	LP4_CSN0_A	LP4X_CSN0_A	--	LP4_CSN0_B	LP4X_CSN0_B	--
LPDDR4 CSN1 A	1T4	LP4_CSN1_A	LP4X_CSN1_A	--	LP4_CSN1_B	LP4X_CSN1_B	--
LPDDR4 CKE0/LPDDR5 CS0 A	1N3	LP4_CKE0_A	LP4X_CKE0_A	LP5_CSN0_A	LP4_CKE0_B	LP4X_CKE0_B	LP5_CSN0_B
LPDDR4 CKE1/LPDDR5 CS1 A	1N5	LP4_CKE1_A	LP4X_CKE1_A	LP5_CSN1_A	LP4_CKE1_B	LP4X_CKE1_B	LP5_CSN1_B



RK3576 BGA698\_16R1X17R2X1R08

## DDR FILTER

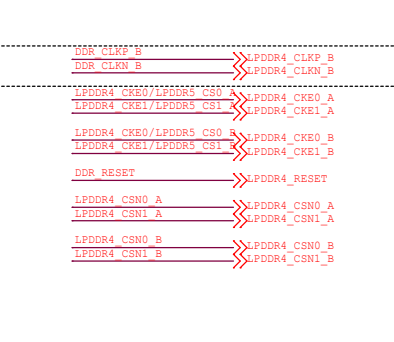
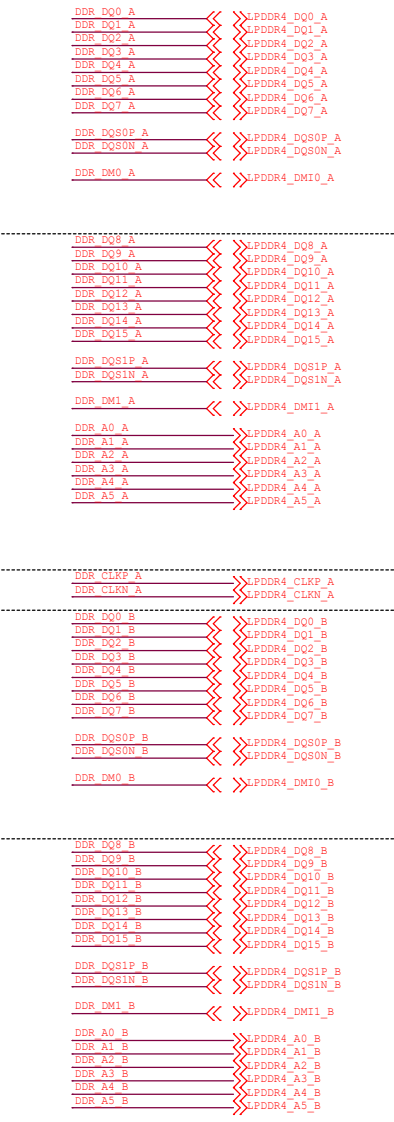


**Note:**  
 (1) Power Sequence: VDD-VDDQ\_CKE-VDDQ  
 (2) Hold power of DDRPHY\_CKE\_VDDQ during retention times.

**Note1:**  
 Caps in the red line dotted box should be placed under the U1000 package

**Note2:**  
 Resistors in the red line dotted box should be placed under the U1000 package

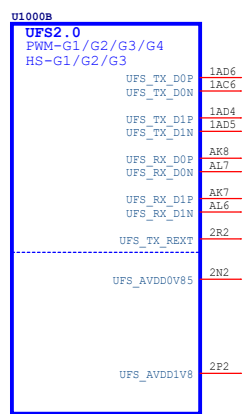
# LPDDR4 Signal



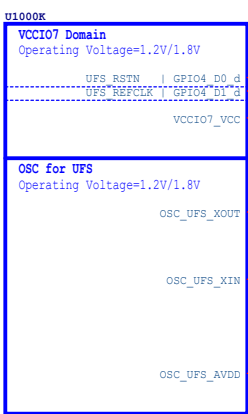
**Rockchip Confidential**  
 Rockchip Electronics Co., Ltd

**Project:** RK\_EVB1\_RK3576\_LP4XD200P132SD6  
**File:** 12.RK3576-DDR PHY  
**Date:** Wednesday, April 01, 2026  
**Designed by:** Wesley Huang **Reviewed by:**   
**Rev:** V1.2  
**Sheet:** 12 of 49

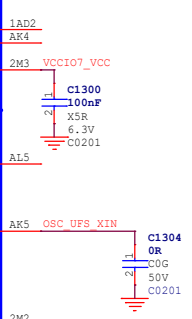
# RK3576 B (UFS2.0)



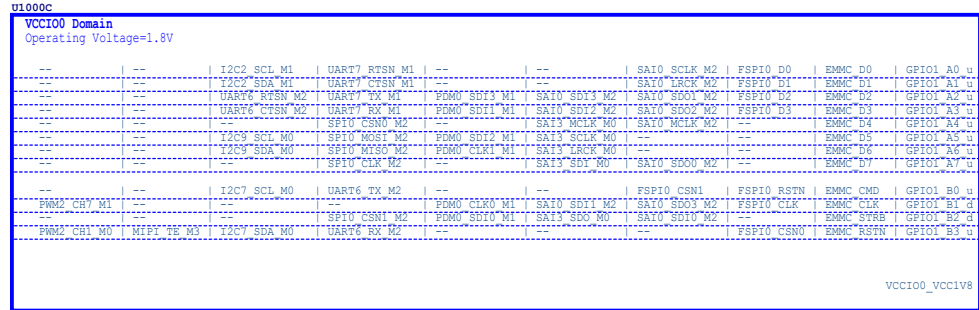
RK3576  
BGA698\_16R1X17R2X1R08



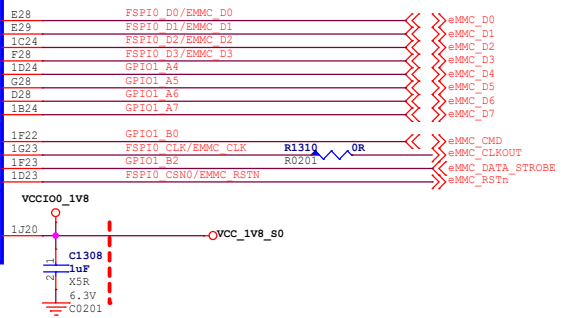
RK3576  
BGA698\_16R1X17R2X1R08



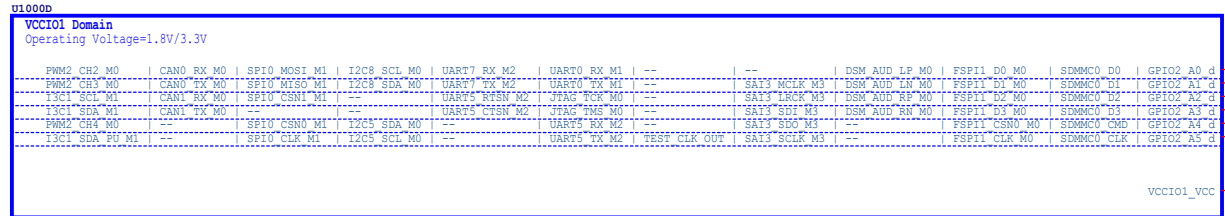
# RK3576 C (VCCIO0)



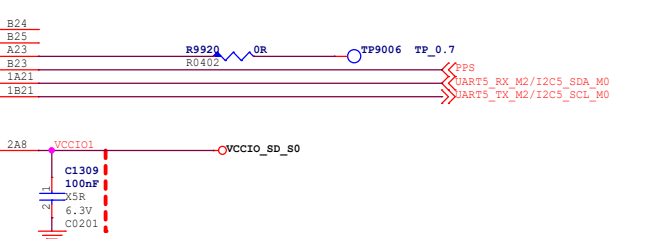
RK3576  
BGA698\_16R1X17R2X1R08



# RK3576 D (VCCIO1)

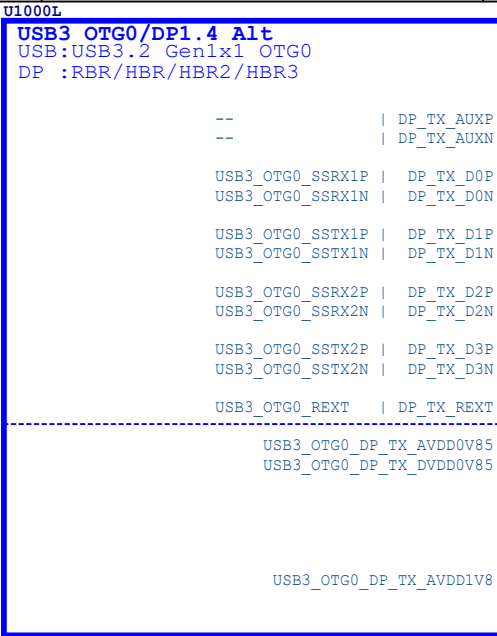


RK3576  
BGA698\_16R1X17R2X1R08



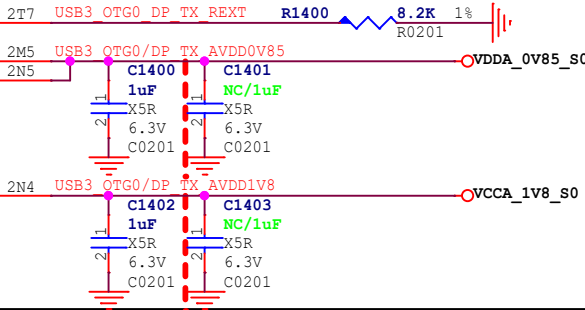
**Note:**  
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

# RK3576 L (USB3/DP)



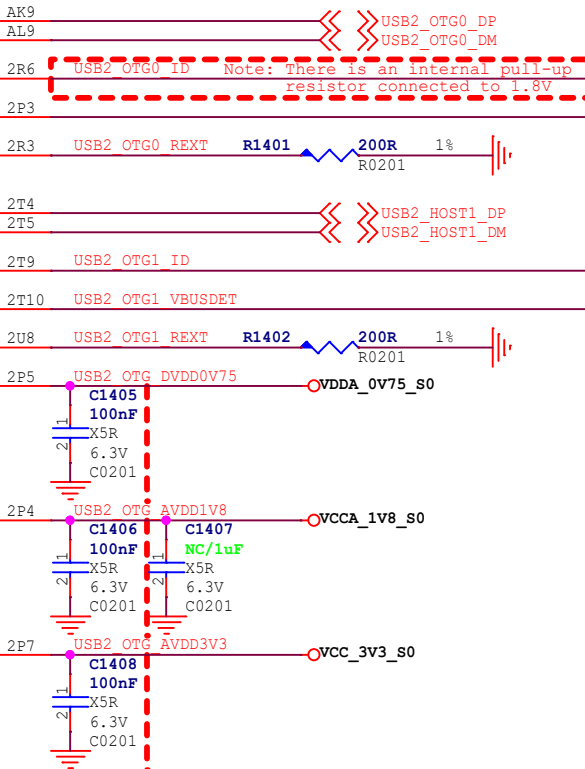
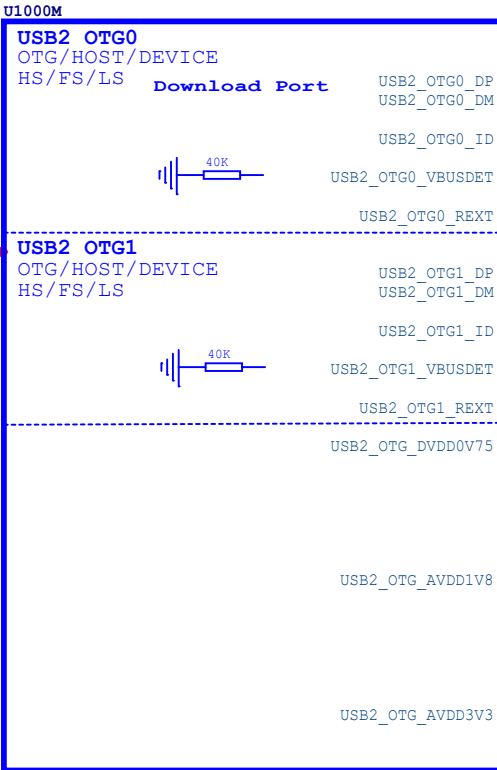
Support:  
Type-C With Displayport Alternate Mode

RK3576  
BGA698\_16R1X17R2X1R08



**Note:**  
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

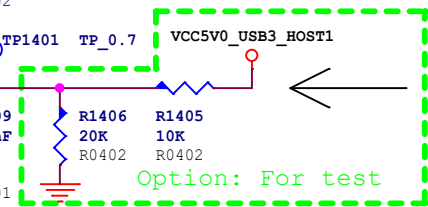
# RK3576 M (USB2)



RK3576  
BGA698\_16R1X17R2X1R08

**Note!!!**  
The USB2 PHY1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

Note: There is an internal pull-up resistor connected to 1.8V

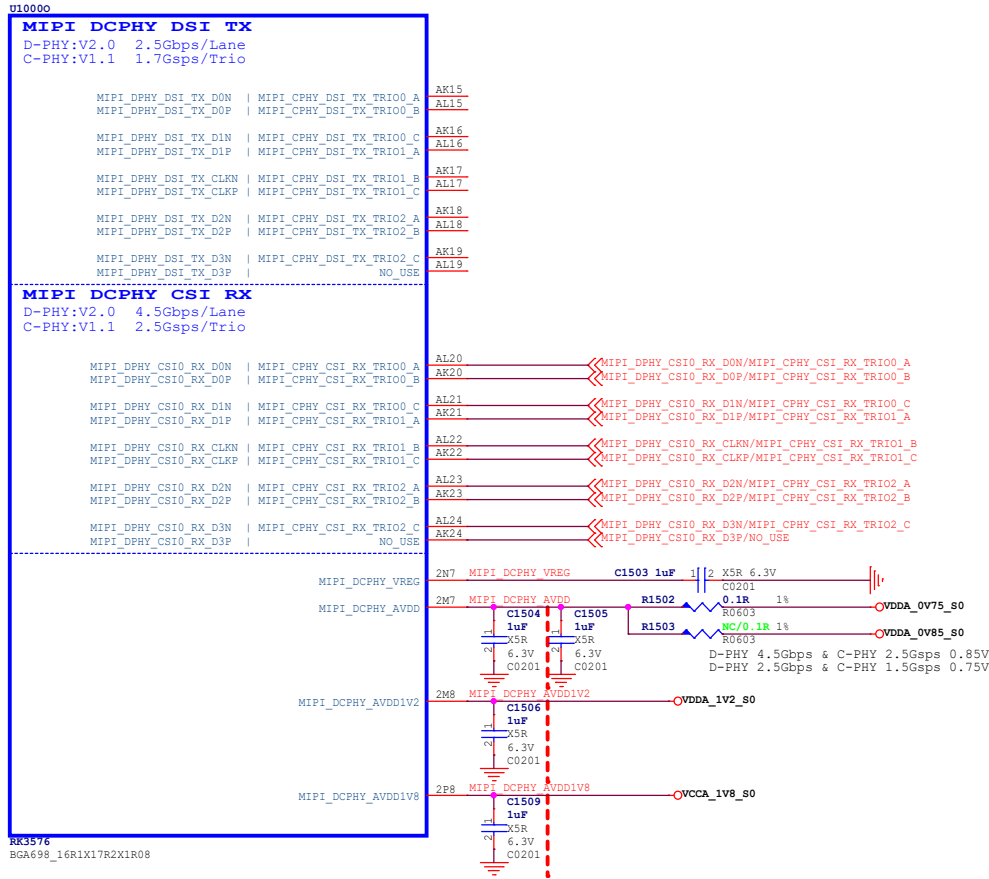


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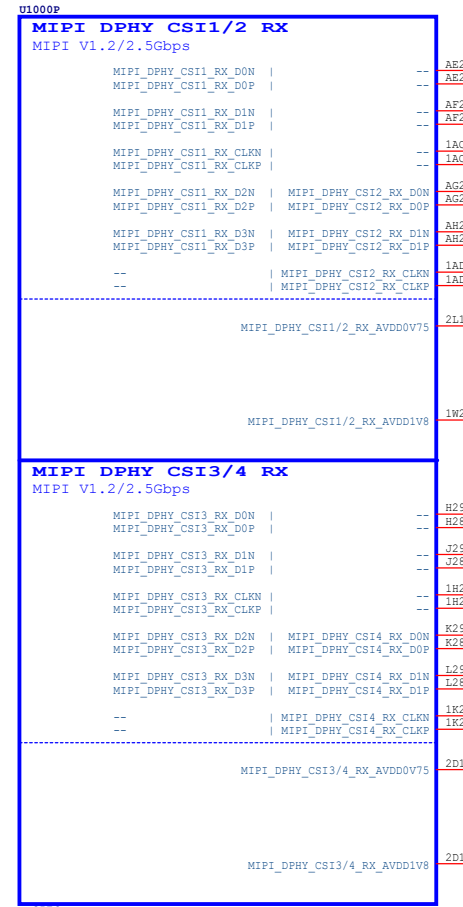
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	14.RK3576-TypeC/USB		
Date:	Wednesday, April 01, 2026	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 14 of 49

# RK3576\_O (MIPI DCPHY)



**Note:**  
 Caps of between dashed red lines and U1000 should be placed under the U1000 package.  
 Other caps should be placed close to the U1000 package

# RK3576\_P (MIPI DPHY CSI RX)



**Note:**  
 Caps of between dashed red lines and U1000 should be placed under the U1000 package.  
 Other caps should be placed close to the U1000 package

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Project:	RK_EVB1_RK3576_LP4XD200P132SD6				
File:	15.RK3576-MIPI DSI/CSI				
Date:	Wednesday, April 01, 2026	Rev:	V1.2		
Designed by:	Wesley Huang	Reviewed by:		Sheet:	15 of 49

# RK3576\_Q (HDMI/eDP)

Note:  
HDMI 2.1 supports up to 4Kx2K@120Hz  
U1000Q

HDMI TX/eDP TX Combo Phy	
HDMI:V2.1	12Gbps
eDP :V1.3	5.4Gbps
HDMI_TX_SBDP   EDP_TX_AUXP	<u>2T12</u>
HDMI_TX_SBDN   EDP_TX_AUXN	<u>2U12</u>
HDMI_TX_D0P   EDP_TX_D0P	<u>1AE24</u>
HDMI_TX_D0N   EDP_TX_D0N	<u>AK27</u>
HDMI_TX_D1P   EDP_TX_D1P	<u>AK28</u>
HDMI_TX_D1N   EDP_TX_D1N	<u>AL28</u>
HDMI_TX_D2P   EDP_TX_D2P	<u>AJ28</u>
HDMI_TX_D2N   EDP_TX_D2N	<u>AK29</u>
HDMI_TX_D3P   EDP_TX_D3P	<u>AL26</u>
HDMI_TX_D3N   EDP_TX_D3N	<u>AK26</u>
HDMI_TX_REXT   EDP_TX_REXT	<u>1AA20</u>
-----	
HDMI_TX_EDP_TX_AVDD0V75	<u>2N11</u>
HDMI_TX_EDP_TX_AVDDC0V75	<u>2P11</u>
-----	
HDMI_TX_EDP_TX_AVDDIO1V8	<u>2N10</u>
HDMI_TX_EDP_TX_AVDDCMN1V8	<u>2P10</u>

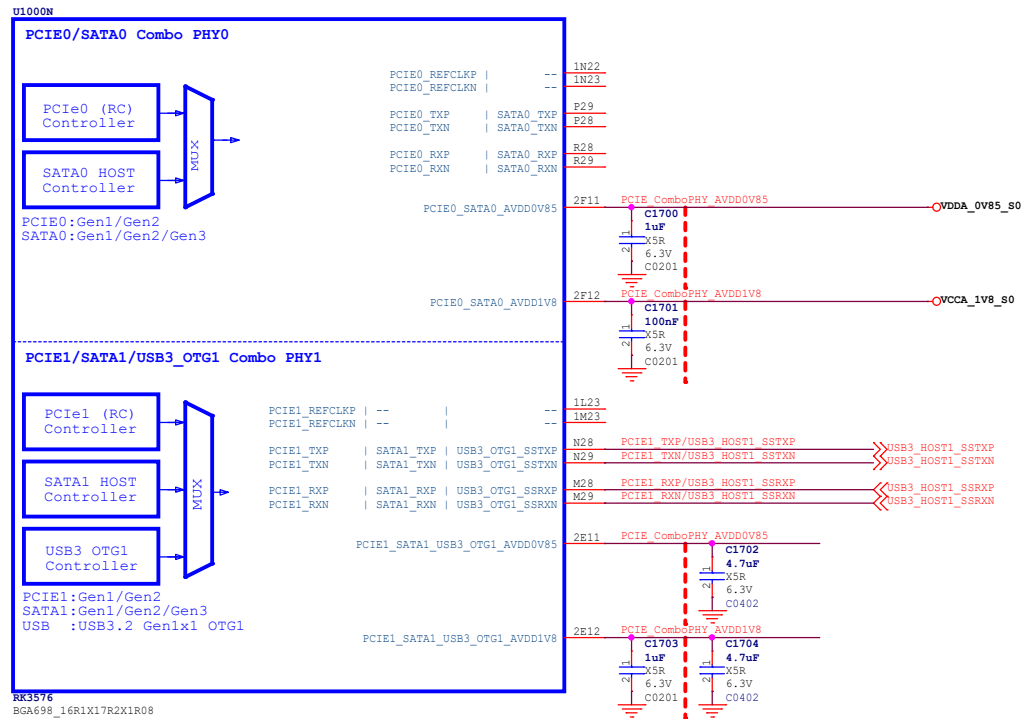
RK3576  
BGA698\_16R1X17R2X1R08

**Note:**  
Caps of between dashed red lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

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<b>Rockchip</b> Rockchip Electronics Co., Ltd	
<b>Project:</b>	RK_EVB1_RK3576_LP4XD200P132SD6
<b>File:</b>	16.RK3576-HDMI/eDP
<b>Date:</b>	Wednesday, April 01, 2026
<b>Designed by:</b>	Wesley Huang
<b>Reviewed by:</b>	
<b>Rev:</b>	V1.2
<b>Sheet:</b>	16 of 49

# RK3576\_N (PCIe/SATA/USB3)



**Note!!!**  
If the PCIe1 or SATA1 function of Combo PHY1 is selected, the USB3 OTG1 function cannot be used, and even the USB2 PHY1 function cannot be used

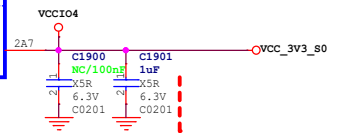
**Note:**  
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package



# RK3576\_H (VCCIO4)

U1000H  
VCCIO4 Domain  
Operating Voltage=1.8V/3.3V

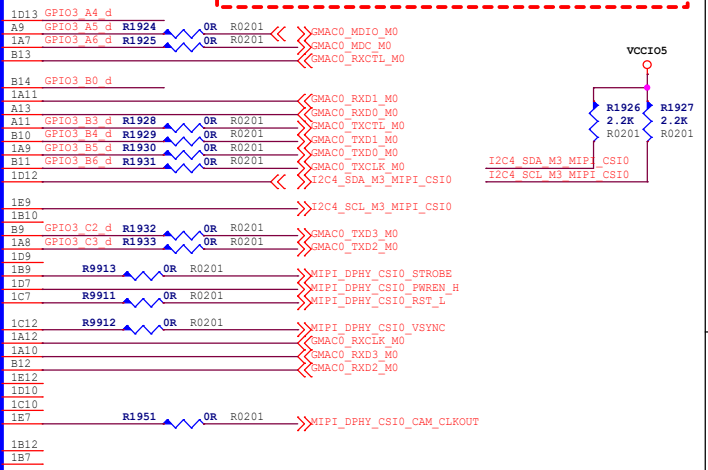
---	---	I2C4_SCL M2	SPI4_CS_N1 M3	UART8_TX M1	---	SATA0_SDO0 M0	ETH0_RXD0 M1	SDMMC1_D0 M1	VI_CIF_D15	GPIO2_A6 d	B22	YPEC_DPTX_AUX_PUPDCTL1
---	---	I2C4_SDA M2	---	UART8_RX M1	---	SATA0_SDI0 M0	ETH0_TXD0 M1	SDMMC1_D1 M1	VI_CIF_D14	GPIO2_A7 d	B20	YPEC_DPTX_AUX_PUPDCTL2
---	---	---	---	UART1_TX M1	PD_M0_SDI3 M3	SATA0_SDI0 M0	ETH0_RXD1 M1	SDMMC1_D2 M1	VI_CIF_D13	GPIO2_B0 d	B19	---
---	---	PCIE0_CLKREQEN M0	SPI4_CS_N0 M3	UART1_RX M1	PD_M0_SDI2 M3	SATA0_SDI1 M0	ETH0_RXD2 M1	SDMMC1_D3 M1	VI_CIF_D12	GPIO2_B1 d	IA18	---
---	---	PCIE1_CLKREQEN M0	SPI4_CS_N1 M3	UART1_RTSN M1	PD_M0_SDI1 M3	SATA0_SDI2 M0	ETH0_RXD3 M1	SDMMC1_D4 M1	VI_CIF_D11	GPIO2_B2 d	IA17	---
---	---	SATA0_ACTIVED M0	SPI4_CLK M3	UART1_RTSN M1	PD_M0_CLK1 M3	SATA0_SDO2 M0	ETH0_RXD4 M1	SDMMC1_CLK M1	VI_CIF_D10	GPIO2_B3 d	IA16	---
---	---	SATA1_ACTIVED M0	SPI4_MOSI M3	UART1_CS_N0 M3	PD_M0_SDI0 M3	SATA0_SDI3 M0	ETH0_RXD5 M1	SDMMC1_PAREN M1	VI_CIF_D9	GPIO2_B4 d	IA15	---
---	---	---	SPI4_MISO M3	UART1_RTSN M1	PD_M0_CLK0 M3	SATA0_SDI4 M0	ETH0_RXD6 M1	SDMMC1_DSEN M1	VI_CIF_D8	GPIO2_B5 d	IA14	MAC0_RSTn
---	---	I2C5_SCL M2	SPI4_CS_N1 M3	UART1_RX M1	---	SATA0_SDI5 M0	ETH0_RXD7 M1	ETH1_PTP_REFCLK M1	VI_CIF_D7	GPIO2_B6 d	A21	---
---	---	I2C5_SDA M2	UART8_CS_N0 M1	UART1_RX M1	---	SATA0_SDI6 M0	ETH0_RXD8 M1	ETH1_CIF_D6	VI_CIF_D6	GPIO2_B7 d	B21	---
---	---	---	---	UART9_RX M0	PD_M1_SDI1 M0	---	---	---	---	GPIO2_C0 d	IA17	---
PWM1_CH0 M2	---	---	SPI1_CS_N1 M1	UART9_RX M0	PD_M1_CLK1 M0	SATA0_MCLK M1	ETH0_PTP_REFCLK M1	ETH1_RXD2 M0	VI_CIF_D5	GPIO2_C1 d	IA15	---
PWM1_CH1 M2	---	---	SPI1_MOSI M1	UART9_RX M0	PD_M1_SDI2 M0	SATA0_SCLK M1	ETH0_PTP_REFCLK M1	ETH1_RXD3 M0	VI_CIF_D4	GPIO2_C2 d	IA15	---
PWM1_CH2 M2	---	---	SPI1_MISO M1	UART11_CS_N1 M1	PD_M1_SDI3 M0	SATA0_SCLK M1	ETH0_PTP_REFCLK M1	ETH1_RXD4 M0	VI_CIF_D3	GPIO2_C3 d	A15	---
PWM1_CH3 M2	---	---	SPI1_CS_N0 M1	UART11_RTSN M1	PD_M1_SDI4 M0	SATA0_SCLK M1	ETH0_PTP_REFCLK M1	ETH1_RXD5 M0	VI_CIF_D2	GPIO2_C4 d	IA13	---
PWM1_CH4 M2	---	---	SPI1_CS_N1 M1	UART11_RX M1	PD_M1_SDI5 M0	SATA0_SCLK M1	ETH0_PTP_REFCLK M1	ETH1_RXD6 M0	VI_CIF_D1	GPIO2_C5 d	IA15	---
PWM1_CH5 M2	---	I2C5_SCL M2	SPI1_CLK M1	UART11_RX M1	PD_M1_CLK0 M0	SATA0_SCLK M1	ETH0_PTP_REFCLK M1	ETH1_RXD7 M0	VI_CIF_D0	GPIO2_C6 d	IA14	---
PWM1_CH6 M2	---	I2C5_SDA M2	---	UART11_RX M1	---	SATA0_SCLK M1	ETH0_PTP_REFCLK M1	ETH1_RXD8 M0	---	GPIO2_C7 d	B15	---
PWM1_CH7 M2	---	---	---	---	---	---	---	---	---	---	---	---
PWM2_CH0 M2	---	I2C6_SCL M2	---	UART4_TX M0	---	SATA4_SDI M3	---	ETH1_RXD9 M0	---	GPIO2_D0 d	B16	---
PWM2_CH1 M2	---	I2C6_SDA M2	---	UART4_RX M0	---	SATA4_SDI M3	---	ETH1_RXD10 M0	---	GPIO2_D1 d	IA16	---
PWM2_CH2 M2	I3C1_SCL M0	---	---	UART4_RX M0	---	SATA4_MCLK M3	---	ETH1_RXD11 M0	CAM_CLK0_OUT M1	GPIO2_D2 d	B17	---
PWM2_CH3 M2	I3C1_SDA M0	---	---	UART4_RX M0	---	SATA4_MCLK M3	---	ETH1_RXD12 M0	CAM_CLK1_OUT M1	GPIO2_D3 d	B18	---
PWM2_CH4 M2	I2C5_SCL M2	---	---	UART4_RTSN M1	---	---	---	ETH1_RXD13 M0	ISP_BRIGHTNESS_HTRIG M0	GPIO2_D4 d	IA13	---
PWM2_CH5 M2	I2C5_SDA M2	---	---	UART4_CS_N0 M1	---	---	---	ETH1_RXD14 M0	ISP_FLASH_TRIGGEROUT M0	GPIO2_D5 d	IA15	---
PWM2_CH6 M2	I3C1_SDA_BU M0	---	---	UART9_RTSN M1	SFP0IF_RX0 M2	SATA3_MCLK M2	ETH0_MCLK M1	ETH_CLK1_25M_OUT M0	CAM_CLK1_OUT M1	GPIO2_D6 d	IA15	---
PWM2_CH7 M2	---	---	SPI3_CS_N1 M0	UART9_CS_N0 M1	SFP0IF_RX0 M2	SATA3_SDO3 M0	ETH0_MCLK M1	ETH1_MCLK M0	CAM_CLK2_OUT M1	GPIO2_D7 d	IA15	---
---	---	I2C7_SCL M1	SPI3_CLK M0	UART3_TX M0	---	SATA3_SCLK M2	ETH0_MCLK M1	---	VI_CIF_HREF	GPIO3_A0 d	IA16	---
---	---	I2C7_SDA M1	SPI3_MOSI M0	UART3_RX M0	---	SATA3_SCLK M2	ETH0_MCLK M1	---	VI_CIF_VSYNC	GPIO3_A1 d	IA18	---
---	---	MIP1_TE M1	SPI3_MISO M0	UART3_CS_N0 M1	SFP0IF_RX1 M1	SATA3_SDO2 M2	ETH0_RXD1 M1	---	VI_CIF_CLK0	GPIO3_A2 d	IA19	---
---	---	CANI_RX M3	SPI3_CS_N0 M1	UART3_RTSN M1	SFP0IF_TX1 M1	SATA3_SDI2 M2	ETH0_RXD2 M1	---	VI_CIF_CLK1	GPIO3_A3 d	IA19	---



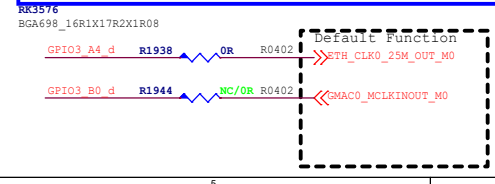
# RK3576\_I (VCCIO5)

U1000I  
VCCIO5 Domain  
Operating Voltage=1.8V/3.3V

PWM1_CH0 M3	---	SPI2_CLK M2	UART1_CS_N2 M2	FLEXBUS0_CS_N0 M1	---	FLEXBUS1_D11	DSMC_RDYN	SATA1_SDI M1	ETH_CLK0_25M_OUT M0	VO_EBC_SDHRR	VO_LCDC_D23	GPIO3_A4 d	1D13 GPIO3 A4 d
PWM1_CH1 M3	---	SPI2_CS_N2 M2	UART1_RTSN M2	---	---	FLEXBUS0_D1	DSMC_DATA15	PWM1_SDI1 M2	ETH0_MCLK M0	VO_EBC_SDSF	VO_LCDC_D22	GPIO3_A5 d	A9 GPIO3 A5 d R1924 OR R0201
PWM1_CH2 M3	---	UART11_RTSN M1	UART1_RX M2	---	---	FLEXBUS0_D5	DSMC_DATA14	PWM1_SDI2 M2	ETH0_MCLK M0	VO_EBC_SDSF	VO_LCDC_D21	GPIO3_A6 d	IA7 GPIO3 A6 d R1925 OR R0201
PWM0_CH0 M3	---	SPI2_MOSI M2	UART10_RX M0	---	---	FLEXBUS0_D8	DSMC_CS_N1	SATA4_MCLK M1	ETH0_MCLK M0	VO_EBC_SDCB3	VO_LCDC_D19	GPIO3_B0 d	B13
PWM0_CH1 M3	---	SPI4_CS_N0 M1	UART9_RX M0	---	---	FLEXBUS0_D4	DSMC_DATA12	ETH0_RXD1 M0	---	VO_EBC_SDCB2	VO_LCDC_D18	GPIO3_B1 d	B14 GPIO3 B0 d
PWM0_CH2 M3	I2C5_SCL M2	---	---	---	---	FLEXBUS0_D3	DSMC_DATA11	PWM1_SDI1 M2	ETH0_RXD2 M0	VO_EBC_SDCB1	VO_LCDC_D17	GPIO3_B2 d	IA11
PWM0_CH3 M3	I2C5_SDA M2	---	---	---	---	FLEXBUS0_D2	DSMC_DATA10	PWM1_SDI2 M2	ETH0_RXD3 M0	VO_EBC_SDCB0	VO_LCDC_D16	GPIO3_B3 d	A13
PWM1_CH4 M3	I2C6_SCL M3	---	---	---	---	FLEXBUS0_D1	DSMC_DATA9	SFP0IF_RX1 M0	ETH0_RXD4 M0	VO_EBC_SDD015	VO_LCDC_D15	GPIO3_B4 d	A11 GPIO3 B3 d R1928 OR R0201
PWM1_CH5 M3	---	SPI3_CS_N0 M1	UART9_CS_N1 M1	---	---	FLEXBUS0_D0	DSMC_DATA8	SFP0IF_TX1 M0	ETH0_RXD5 M0	VO_EBC_SDD014	VO_LCDC_D14	GPIO3_B5 d	B10 GPIO3 B4 d R1929 OR R0201
PWM1_CH6 M3	I2C4_SDA M1	SPI3_CS_N1 M1	---	---	---	FLEXBUS0_CLK	DSMC_DDS1	---	---	VO_EBC_SDD013	VO_LCDC_D13	GPIO3_B6 d	IA9 GPIO3 B5 d R1930 OR R0201
PWM1_CH7 M3	I2C4_SDA M1	UART3_CS_N1 M1	UART2_RX M2	FLEXBUS1_CS_N0 M1	---	FLEXBUS1_D10	DSMC_DDS0	SATA1_SDI0 M1	ETH0_PTP_REFCLK M0	VO_EBC_SDD012	VO_LCDC_D12	GPIO3_B7 d	B11 GPIO3 B6 d R1931 OR R0201
---	I2C4_SCL M3	UART3_RTSN M1	UART2_TX M2	---	---	FLEXBUS1_D9	DSMC_DATA7	SATA1_SDO3 M1	ETH0_PTP_REFCLK M0	VO_EBC_SDD011	VO_LCDC_D11	GPIO3_B8 d	IA12
CANI_RX M3	I2C5_SDA M2	SPI2_CS_N2 M2	UART11_RX M0	---	---	FLEXBUS1_D8	DSMC_DATA6	SATA1_SDO2 M1	ETH0_PTP_REFCLK M0	VO_EBC_SDD010	VO_LCDC_D10	GPIO3_C0 d	1E9
PWM2_CH0 M3	I2C5_SCL M2	SPI4_MOSI M1	UART11_RTSN M0	---	---	FLEXBUS1_D7	DSMC_DATA5	SATA1_SDI1 M2	ETH0_RXD1 M0	VO_EBC_SDD009	VO_LCDC_D9	GPIO3_C1 d	B9 GPIO3 C2 d R1932 OR R0201
PWM2_CH1 M3	I2C5_SDA M2	SPI4_MISO M1	UART11_CS_N0 M1	FLEXBUS0_CS_N2 M1	---	FLEXBUS1_D10	DSMC_DATA4	SATA1_SDI2 M2	ETH0_RXD2 M0	VO_EBC_SDD008	VO_LCDC_D8	GPIO3_C2 d	IA8 GPIO3 C3 d R1933 OR R0201
CANI_RX M3	I2C5_SCL M2	SPI2_CS_N0 M2	UART9_CS_N0 M1	---	---	FLEXBUS1_D7	DSMC_DATA3	SATA1_SDO1 M1	---	VO_EBC_SDD007	VO_LCDC_D7	GPIO3_C4 d	1B9 R9913 OR R0201
PWM2_CH2 M3	---	SPI1_MISO M2	UART9_RX M0	---	---	FLEXBUS1_D6	DSMC_DATA4	SATA1_SDO0 M1	---	VO_EBC_SDD006	VO_LCDC_D6	GPIO3_C5 d	1D7
PWM2_CH3 M3	---	SPI1_MOSI M2	UART9_CS_N0 M1	---	---	FLEXBUS1_D5	DSMC_DATA3	SATA1_LRCK M1	---	VO_EBC_SDD005	VO_LCDC_D5	GPIO3_C6 d	1C7 R9911 OR R0201
PWM2_CH4 M3	---	SPI1_CLK M2	UART9_RTSN M0	---	---	FLEXBUS1_D4	DSMC_DATA2	SATA1_LRCK M1	---	VO_EBC_SDD004	VO_LCDC_D4	GPIO3_C7 d	1C12
PWM2_CH5 M3	---	SPI1_CS_N0 M2	UART9_CS_N0 M1	---	---	FLEXBUS1_D3	DSMC_DATA1	SATA1_MCLK M1	---	VO_EBC_SDD003	VO_LCDC_D3	GPIO3_D0 d	1C11 R9912 OR R0201
PWM2_CH6 M3	I3C1_SDA_BU M0	SPI4_CLK M1	---	FLEXBUS1_CS_N2 M1	---	FLEXBUS0_D11	DSMC_CS_N2	SATA2_MCLK M1	---	VO_EBC_SDD002	VO_LCDC_D2	GPIO3_D1 d	IA12
PWM2_CH7 M3	I3C1_SDA M0	SPI4_CS_N1 M1	UART2_RTSN M2	FLEXBUS0_CS_N1 M1	FLEXBUS1_D15 M0	FLEXBUS0_D12	DSMC_CS_N3	SATA2_SDI2 M2	ETH0_RXD3 M0	VO_EBC_SDD001	VO_LCDC_D1	GPIO3_D2 d	B10
PWM2_CH8 M3	I3C1_SCL M2	---	---	---	---	FLEXBUS0_D2	DSMC_CS_N0	SATA2_SDI1 M2	ETH0_RXD4 M0	VO_EBC_SDD000	VO_LCDC_D0	GPIO3_D3 d	1E12
PWM2_CH9 M3	I2C5_SCL M2	SPI2_CS_N1 M1	UART3_RX M0	---	---	FLEXBUS1_D1	DSMC_DATA0	SATA1_SDI1 M2	---	VO_EBC_SDL1	VO_LCDC_DEN	GPIO3_D4 d	1D10
PWM2_CH10 M3	I2C5_SDA M2	SPI2_CS_N0 M1	UART3_CS_N0 M1	---	---	FLEXBUS1_D0	DSMC_CLKA	SATA1_SDI0 M1	---	VO_EBC_SDL0	VO_LCDC_HSVDEN	GPIO3_D5 d	1C10
PWM2_CH11 M3	---	SPI3_MOSI M1	UART3_CS_N0 M1	FLEXBUS1_CS_N1 M1	FLEXBUS1_D12 M0	FLEXBUS0_D13 M0	DSMC_CLKB	SATA1_SDI1 M2	CAM_CLK0_OUT M0	VO_EBC_SDL0	VO_LCDC_CLK	GPIO3_D6 d	1E7
PWM2_CH12 M3	---	SPI3_CS_N1 M1	UART3_RTSN M0	FLEXBUS1_CS_N1 M1	FLEXBUS1_D12 M0	FLEXBUS0_D13 M0	DSMC_CLKA	SATA1_SDI1 M2	CAM_CLK0_OUT M0	VO_EBC_SDL0	VO_LCDC_CLK	GPIO3_D7 d	1B12
MIP1_TE M2	I2C7_SCL M2	SPI1_CS_N1 M2	UART3_TX M0	FLEXBUS1_CS_N3 M1	FLEXBUS1_D14 M0	FLEXBUS0_D13 M0	DSMC_INFO	SATA4_LRCK M1	CAM_CLK1_OUT M0	SFP0IF_RX0 M1	---	GPIO4_A0 d	1B7
PWM2_CH13 M3	I2C7_SDA M2	---	UART3_RX M0	FLEXBUS1_CS_N1 M1	FLEXBUS1_D13 M0	FLEXBUS0_D14 M0	DSMC_INFO	SATA3_SDO1 M1	CAM_CLK2_OUT M0	SFP0IF_RX0 M1	VO_PDSH_EMPTY	GPIO4_A1 d	---



**Note:**  
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package



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Project: RK\_EVB1\_RK3576\_LP4XD200P132SD6  
File: 19.RK3576-GPIO VCCIO4/5  
Date: Wednesday, April 01, 2026  
Designed by: Wesley Huang

Rev: V1.2  
Reviewed by: [ ]  
Sheet: 19 of 49

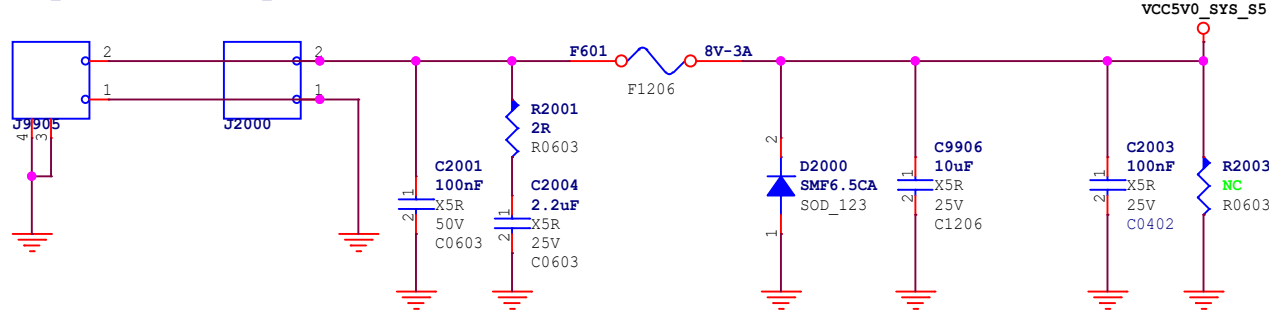
# 5V IN

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CONN-TH\_B2B-PH-K-S

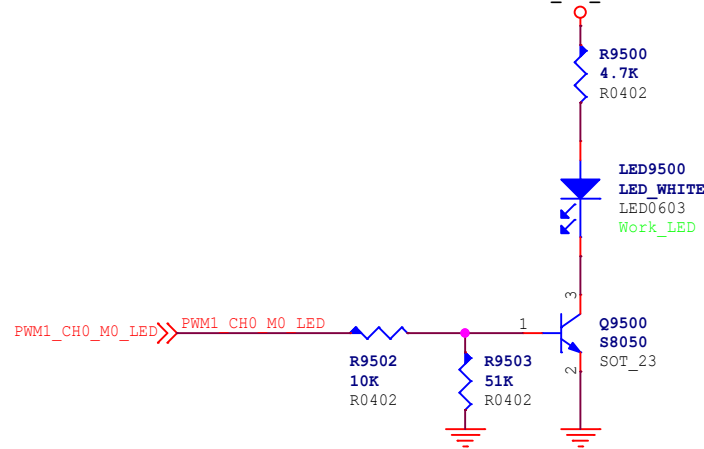
2PIN\_ZH1.5MM

2PIN\_PH2.0MM

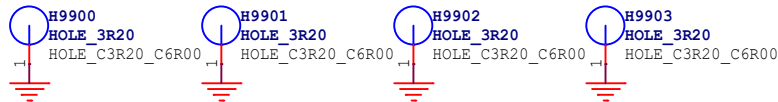


VCC5V0\_SYS\_S5

# VCC5V0\_SYS



# Hole



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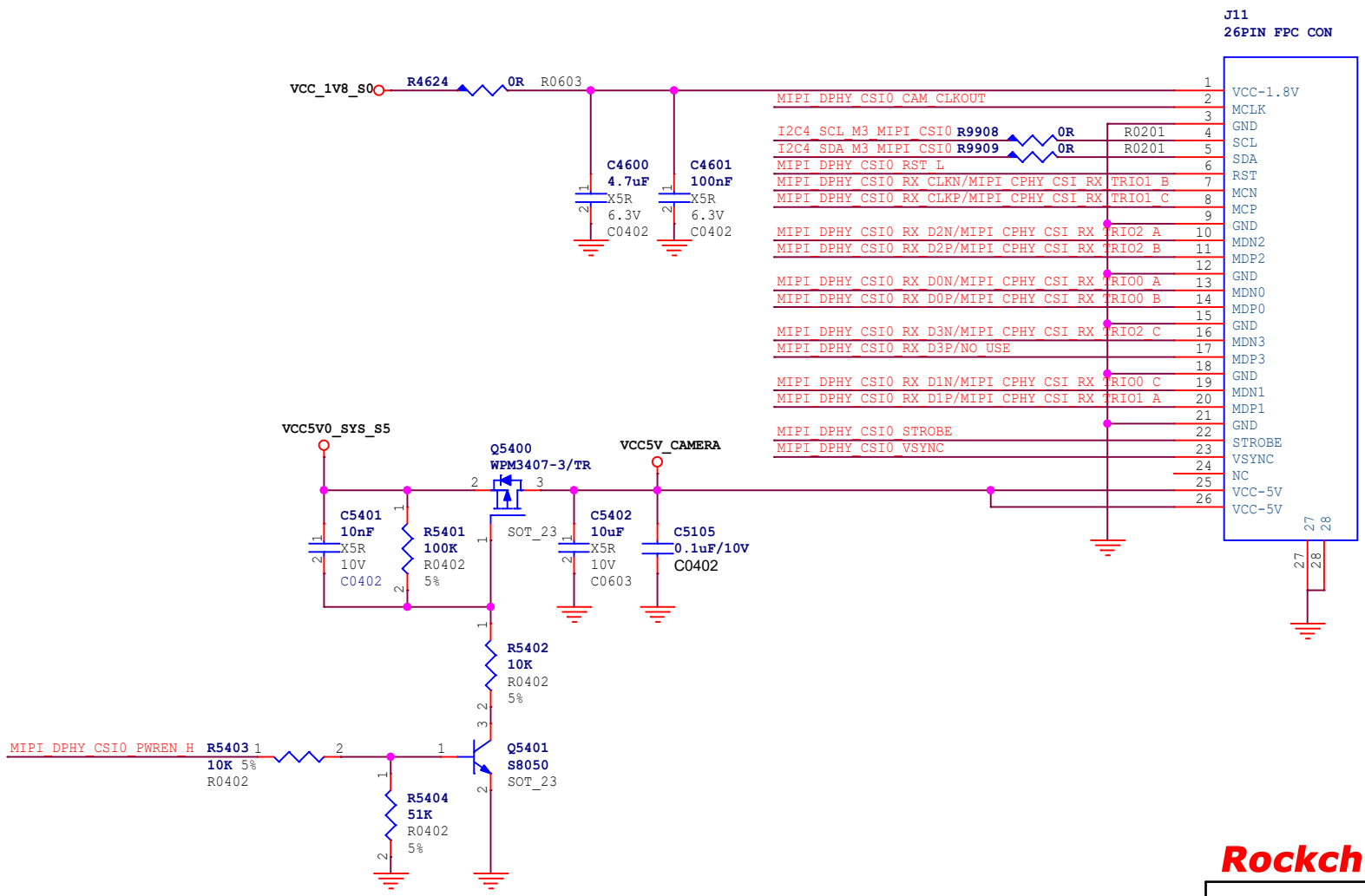
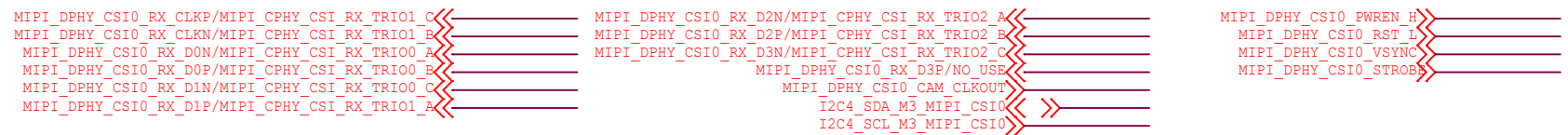
Project:	RK_EVB1_RK3576_LP4XD200P132SD6		
File:	20.Power-DC IN		
Date:	Wednesday, April 01, 2026	Rev:	V1.2
Designed by:	Wesley Huang	Reviewed by:	Sheet: 20 of 49







# MIPI-CSIO\_RX



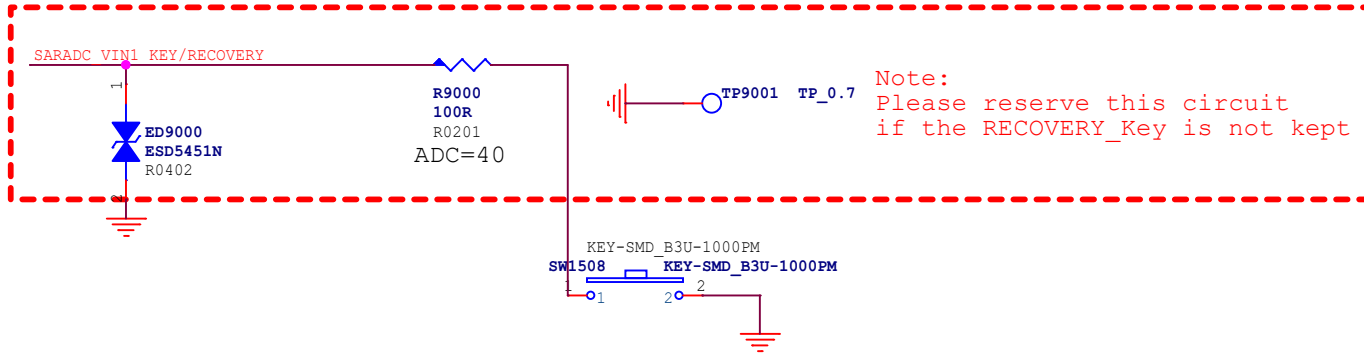
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<b>Rockchip</b> Rockchip Electronics Co., Ltd	
<b>Project:</b>	RK_EVB1_RK3576_LP4XD200P132SD6
<b>File:</b>	46.VI-Camera_MIPI-DCPHY
<b>Date:</b>	Wednesday, April 01, 2026
<b>Reviewed by:</b>	Wesley Huang
<b>Rev:</b>	V1.2
<b>Sheet:</b>	29 of 49

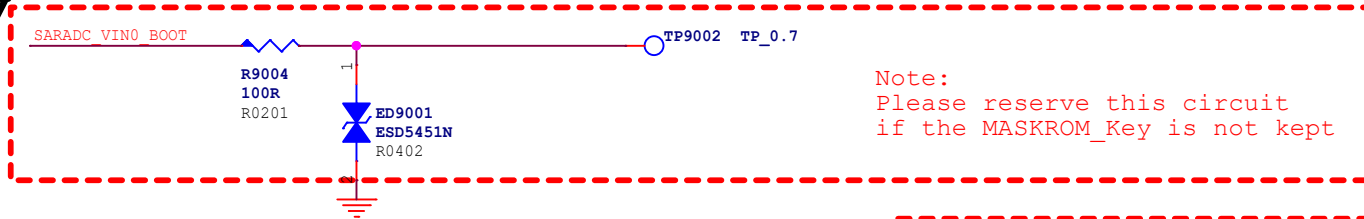


SARADC\_VIN1\_KEY/RECOVERY  
 RESET\_L  
 PWRON\_L  
 SARADC\_VIN0\_BOOT

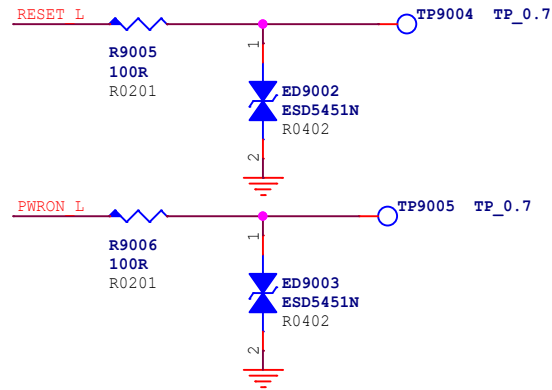
# KEY



# MASKROM Key



**Note:**  
 If SARADC\_VIN0\_BOOT=0V after power-on reset, then system will enter into MASKROM mode.



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<b>Project:</b>	RK_EVB1_RK3576_LP4XD200P132SD6
<b>File:</b>	90.Key-PowerON/Reset/V+/V-/etc
<b>Date:</b>	Wednesday, April 01, 2026
<b>Designed by:</b>	Wesley Huang
<b>Reviewed by:</b>	
<b>Rev:</b>	V1.2
<b>Sheet:</b>	42 of 49

UART0\_RX\_M0\_DEBUG  
 UART0\_TX\_M0\_DEBUG  
 PPS  
 UART5\_TX\_M2/I2C5\_SCL\_M0  
 UART5\_RX\_M2/I2C5\_SDA\_M0

# Debug UART\_M0

