深圳市一众显示科技有限公司

SHEN ZHEN TEAM SOURCE DISPLAY TECH. CO, TD.

TFT-LCD Module Specification

Module NO.: TST320FHCT-01

Version: V1.0

☐ APPROVAL FOR SPECIFICATION ☐ APPROVAL FOR SAMPLE

For Customer's Acceptance:	
Approved by	Comment

Team Source Display:		
Presented by	Reviewed by	Organized by

Version No.	Date	Content	Remark
V1.0	2021-10-05	First Released	

Contents

1. GENERAL DESCRIPTION

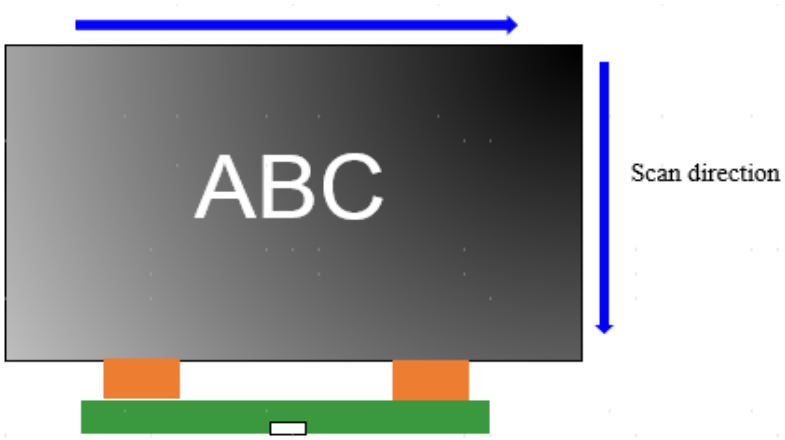
The specification is applied to 31.5” model (TST320FHCT-01) TFT Liquid Crystal Display module and it supports 1920×1080 FHD mode with 16.7M colors. This product is with driver ICs and a 51-pins-2ch-LVDS circuit board and built in with backlight unit.

1.1 General Specifications

Item	Specification	Unit	Note
Screen Size	31.5 inch Diagonal	inch	-
Outline Dimension	715(H) x 411(V)	mm	
Active area	698.40 (H) x 392.85 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Cell transmittance	5.5	%	HKC BLU，center point
Pixel Number	1920×1080	pixel	-
Sub Pixel Pitch	363.75(H)x121.25(V)	um	-
Pixel Arrangement	RGB Horizontal	-	-
Display Colors	16.7M	color	-
Display Mode	Normally Black	-	-
Display Orientation	Signal input with “ABC”	-	(1)
Surface Treatment	Type=AG	-	-
	Haze=3%		
	Top Surface Hardness 3H	-	
Weight	924.4	g	

Note:

(1)



2. ABSOLUTE MAXIMUM RATINGS

2.1 Absolute Maximun Ratings

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Input Signal Voltage	V_{in}	-0.3	3.6	V	(1)

Note:

(1) Within Ta=25±2℃

2.2 Absolute Ratings of Environment

Temperature and relative humidity range is shown in the figure below.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	60	℃	(1)
Operating Temperature	TOP	0	50	℃	(1), (2), (3)

Note:

(1) a. 90 % RH Max. (Ta ≤ 40 °C).

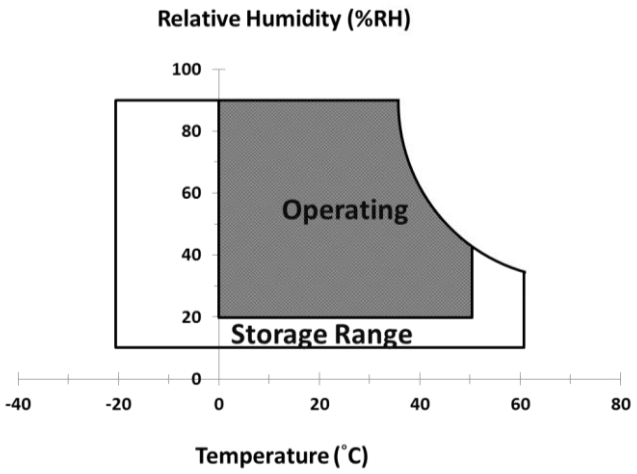
b. Web-bulb temperature should be 39℃ Max.(Ta>40 ℃)

c. No condensation

d. Operating condition with a assemble module

(2) The temperature of panel surface should be 0 ℃ min. and 50 ℃ max.

(3) Any point on the Driver surface must be less than 120 ℃ under any condition. Module designer should apply adequate thermal solutions to keep the electrical components surface temperature under control limit (ex: Source Driver IC 120 ℃, Components on T-con PCB 100 ℃). Operation over the temperature can cause damages or decrease of life time.



3. ELECTRICAL SPECIFICATIONS

3.1 Electrical Characteristics

3.1.1 Power Consumption

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(2)
Rush Current		I_{RUSH}	-	-	TBD	A	(3)
Power Supply Current	**White Pattern**	-	-	TBD	TBD	A	(4)
	Horizontal Stripe	-	-	TBD	TBD	A	
	Black Pattern	-	-	TBD	TBD	A	

Note:

(1) Ambient temperature: 25 ±2℃

(2) The ripple voltage should be controlled under 10% of VCC.

(3) Measurement Conditions: VCC rising time=470μs.

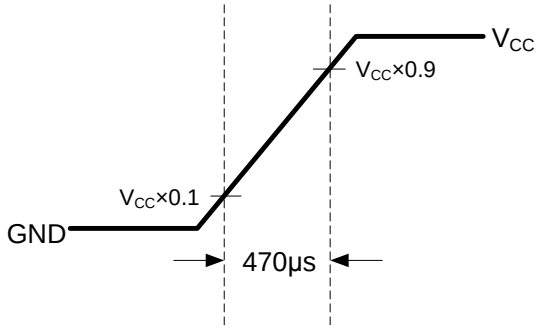


Fig 3.1 VCC rising time condition

(4) Measurement Conditions: Vcc =12V, Ta = 25 ±2 ℃, Fv = 60 Hz, whereas the test pattern is shown as below.

A. White Pattern B. Horizontal Strip C. Black Pattern

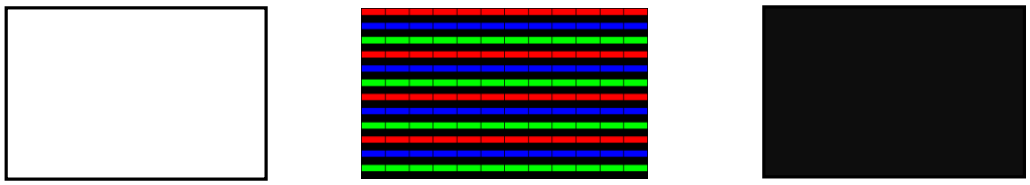


Fig 3.2 Test pattern

3.1.2 LVDS Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS interface	Differential Input High Threshold Voltage	V_{TH}	+100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	90	100	110	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.6	V	

Note:

(1) The LVDS input signal has been defined as follows:

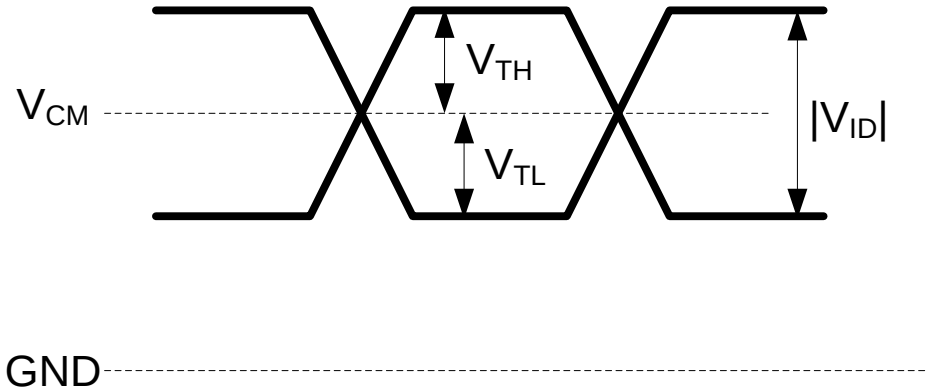


Fig 3.3 LVDS input signal

3.1.3 LVDS Format

VESA Format: SELLVDS = H or Open

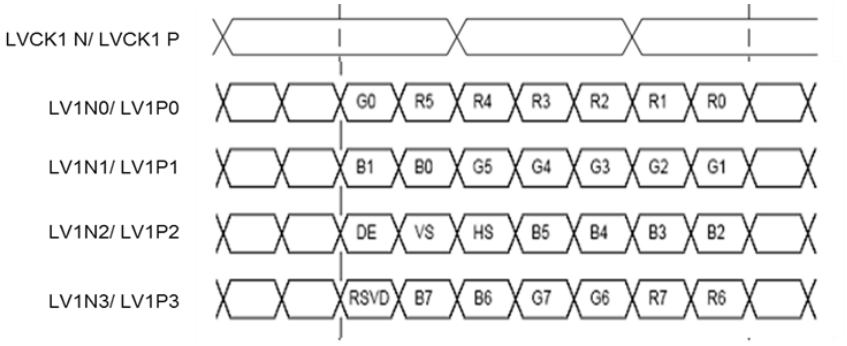


Fig 3.4 VESA format

JEIDA Format: SELLVDS = L

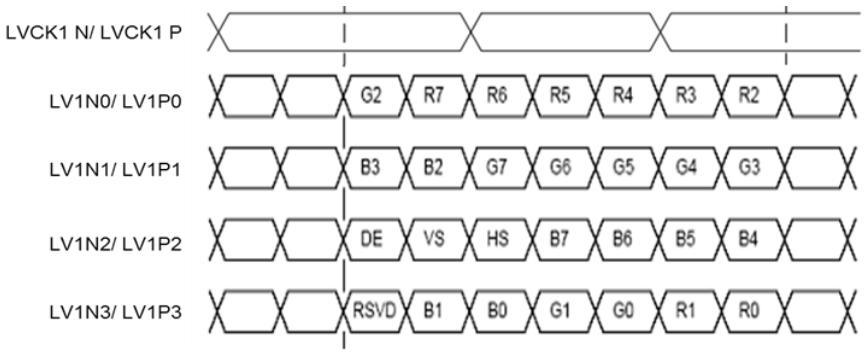


Fig 3.5 JEIDA format

3.1.4 Block Diagram

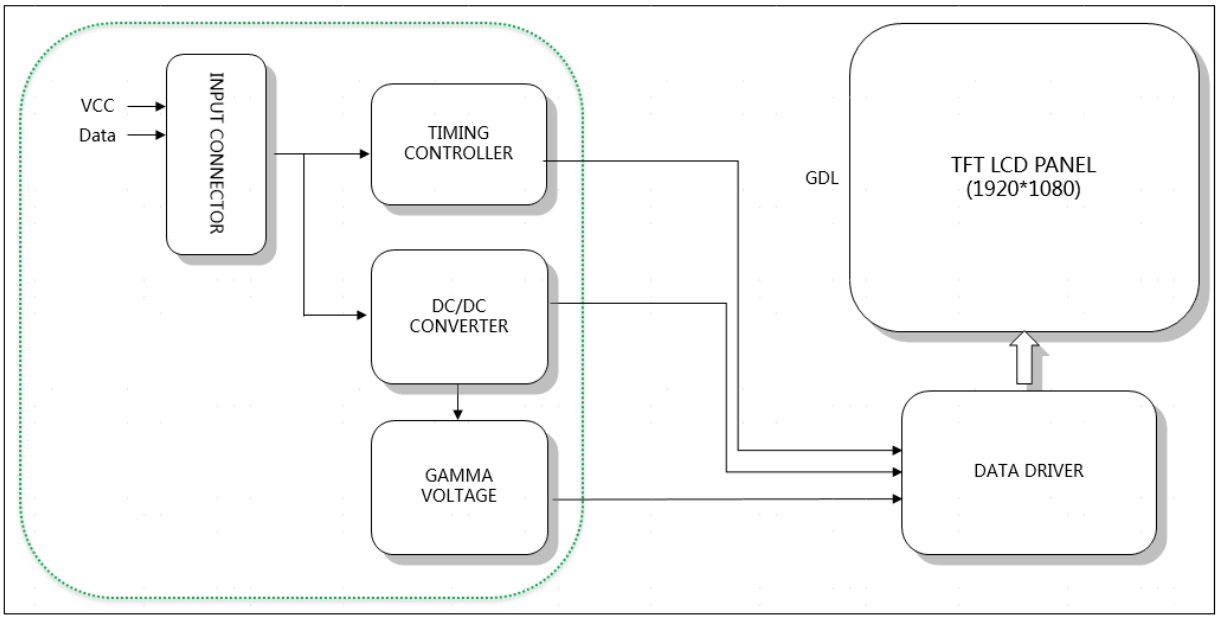


Fig 3.6 Block diagram

3.2 Interface Connections

3.2.1 Interface Pin Assignment

Connector part No.: CN1 F05035-51P-U (CT) or equivalent 0.5mm pitch 51 pin (1).

Pin No.	Symbol	Description	Note
1	WP	White Protection	(2)
2	SCL	I2C Clock	
3	SDA	I2C Data	
4	NC	NO connection	
5	NC	NO connection	
6	NC	NO connection	
7	LVDS_SEL	LVDS data format selection	(3)
8	NC	No connection	
9	BIST_MODE	Select BIST Mode	(4)
10	NC	No connection	
11	GND	Ground	
12	LV1N0	LVDS Channel 1, Signal 0-	
13	LV1P0	LVDS Channel 1, Signal 0+	
14	LV1N1	LVDS Channel 1, Signal 1-	
15	LV1P1	LVDS Channel 1, Signal 1+	
16	LV1N2	LVDS Channel 1, Signal 2-	
17	LV1P2	LVDS Channel 1, Signal 2+	
18	GND	Ground	
19	LV1CLKN	LVDS Channel 1, Clock-	
20	LV1CLKP	LVDS Channel 1, Clock+	
21	GND	Ground	
22	LV1N3	LVDS Channel 1, Signal 3-	
23	LV1P3	LVDS Channel 1, Signal 3+	
24	NC	No connection	
25	NC	No connection	
26	NC	No connection	
27	NC	No connection	
28	LV2N0	LVDS Channel 2, Signal 0-	
29	LV2P0	LVDS Channel 2, Signal 0+	
30	LV2N1	LVDS Channel 2, Signal 1-	
31	LV2P1	LVDS Channel 2, Signal 1+	
32	LV2N2	LVDS Channel 2, Signal 2-	

33	LV2P2	LVDS Channel 2, Signal 2+	
34	GND	Ground	
35	LV2CLKN	LVDS Channel 2, Clock-	
36	LV2CLKP	LVDS Channel 2, Clock+	
37	GND	Ground	
38	LV2N3	LVDS Channel 2, Signal 3-	
39	LV2P3	LVDS Channel 2, Signal 3+	
40	NC	No connection	
41	NC	No connection	
42	NC	No connection	
43	NC	No connection	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	NC	No connection	
48	VDD	Power Supply Input Voltage	
49	VDD	Power Supply Input Voltage	
50	VDD	Power Supply Input Voltage	
51	VDD	Power Supply Input Voltage	

Note:

(1) Following finger shows the LVDS pin1 diagram.

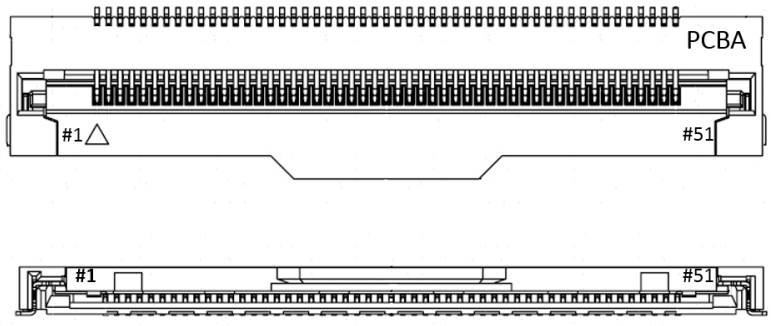


Fig 3.7 LVDS connector direction sketch map

(2) WP pull high/low setting:

L = Connect to GND, H =Connect to +3.3V.

WP	Note
L or Open	Write Disable
H	Write Enable

(3) SELLVDS pull high/low setting:

L = Connect to GND, H =Connect to +3.3V

LVDS_SEL	Note
H or Open	VESA
L	JEIDA

(4) BIST_MODE pull high/low setting:

L=Connect to GND,H=Connect to +3.3V

BIST_MODE	Note
L or Open	Normal
H	BIST Mode

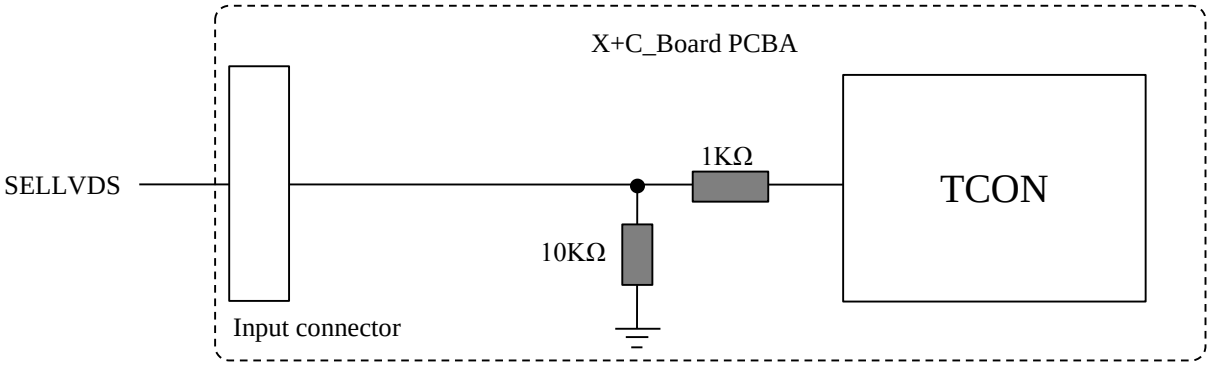
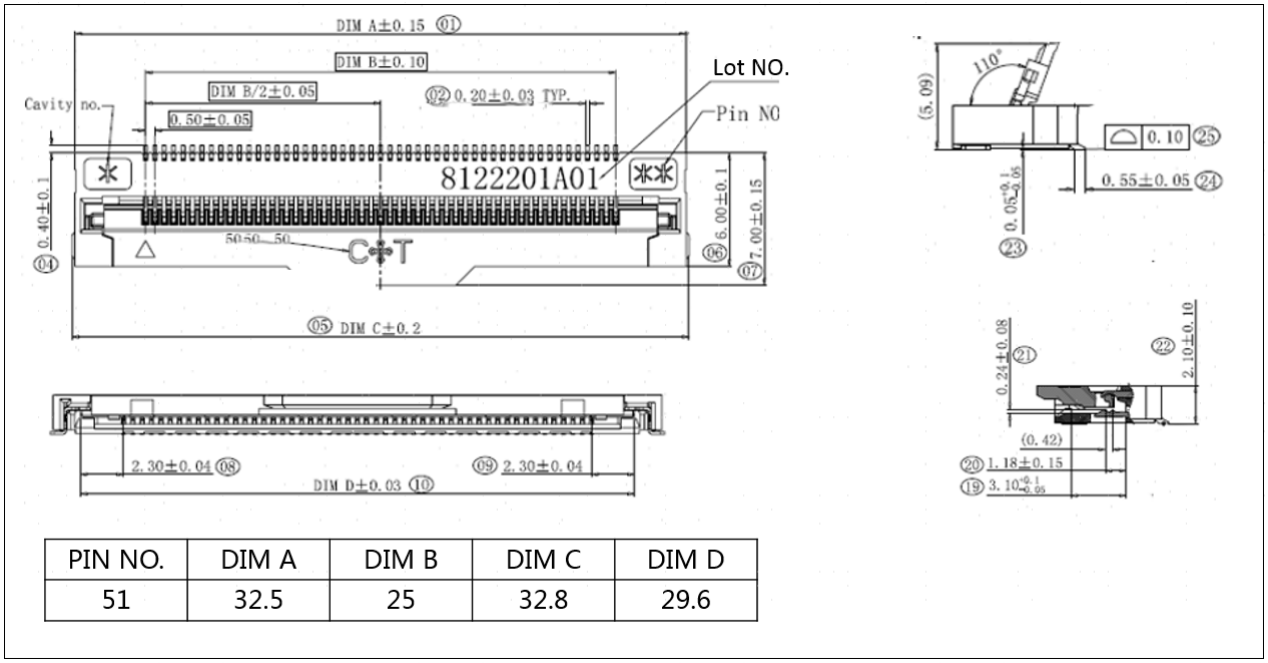


Fig.3.8 WP/SDA/SCL PCBA set

(5) Connector drawing.



PIN NO.	DIM A	DIM B	DIM C	DIM D
51	32.5	25	32.8	29.6

Fig.3.9 Connector drawing

3.3 Timing Specification

The input signal timing specifications are shown as the following table and timing diagram.

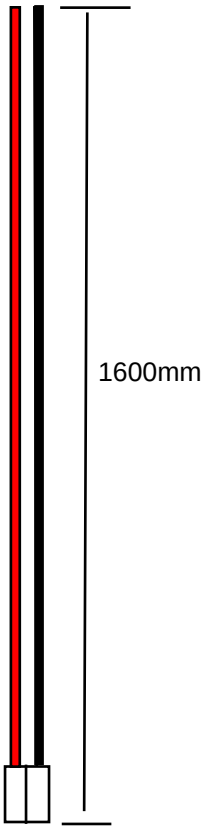
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	F_{clkin}	65	74.25	80	MHz	(1)
	Input cycle to cycle jitter	Trcl	—	—	200	ps	(2)
	Spread spectrum modulation range	Fclkin_mod	Fclkin-2%	—	Fclkin+2%	MHz	(3)
	Spread spectrum modulation frequency	FSSM	—	—	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	TRSM	-400	—	400	ps	(4)
Vertical Term	Frame Rate	F	48	60	62.5	Hz	
	Total	TV	1092	1125	1380	T_H	$T_V = T_{VD} + T_{VB}$
	Active Display	TVD	1080			T_H	
	Blank	TVB	12	45	300	T_H	
Horizontal Term	Total	TH	1046	1100	1174	T_{CLK}	$T_H = T_{HD} + T_{HB}$
	Active Display	THD	960			T_{CLK}	
	Blank	THB	86	140	214	T_{CLK}	

(Ta)＝25℃±2　　湿度 HR=65%±10

Item			unit	Spction			Remark
				MIN	TYP	MAX	
1	BLU Brightness	Center point	cd/m^2	270	300	---	Center point （NOTE 1）
	Uniformity	9 点		72%	75%	---	（NOTE2）
2	LCM CIE	x	---	-0.030	0.297	+0.030	Center point
		y	---	-0.030	0.317	+0.030	Center point

Item	Symbol	Condition	Values			Unit	Remark
			MIN	TYP	MAX		
Input lightbar votage	V_{pin}	single	45	48	49.5	V	NOTE 1/2
Input lightbar current	I_{pin}	single	---	640		MA	
Led life Time	Hours	-----	25000	-----	-----		

LED Strip pin: TSD using 4014 LED(90mA) 18x8 LEDs RED line is V+ & Black line is V-



Attention:

The module is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.

Note:

(1) Please make sure the range of pixel clock follows the following equations:

$F_{CLK}(max) \geq F_{max} \times T_V \times T_H$ $F_{CLK}(min) \leq F_{min} \times T_V \times T_H$

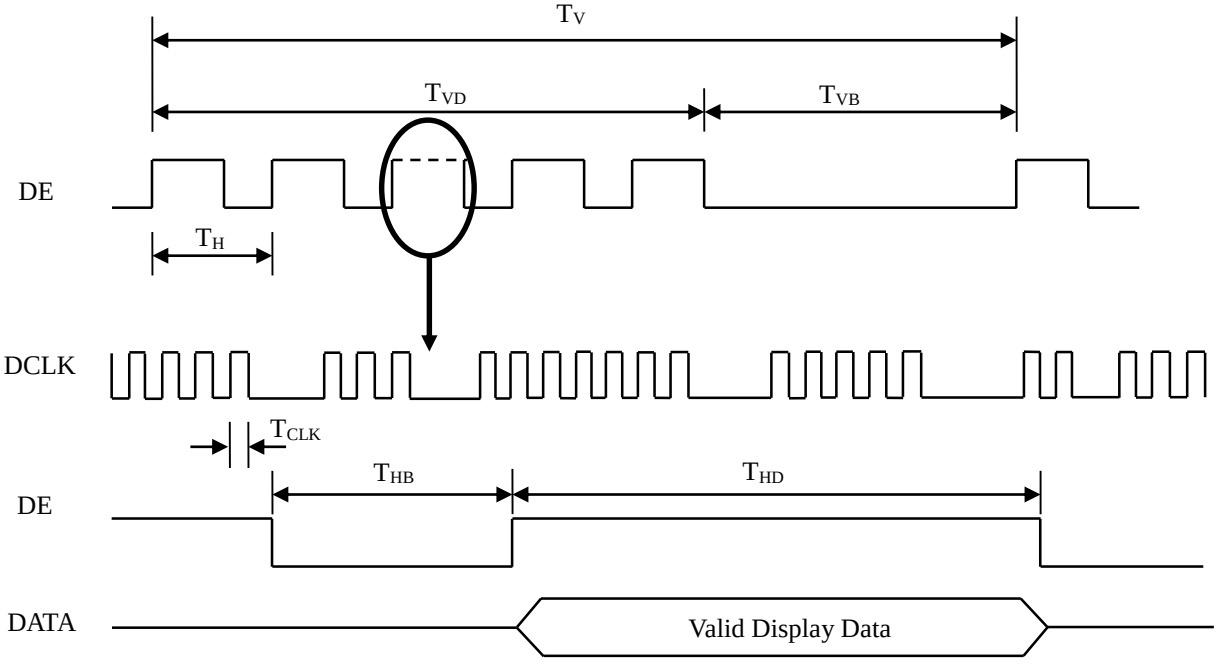


Fig 3.10 Signal timing diagram

(2) The input clock cycle-to-cycle is defined as below figures.

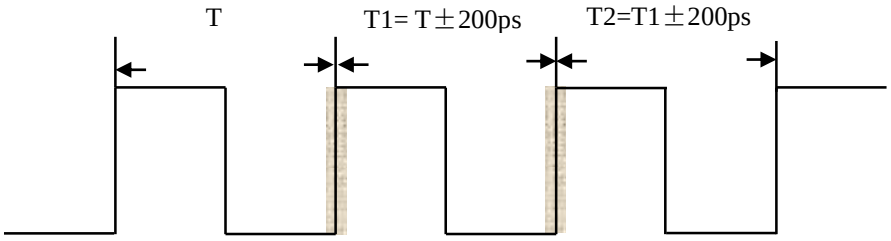


Fig 3.11 Jitter

(3) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure.

The LVDS SSM's suggestion is off by default, SOC board must test all validation if SOC board open the LVDS SSM.

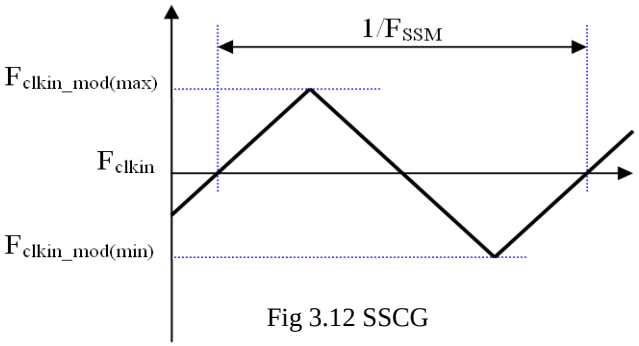


Fig 3.12 SSCG

(4) The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

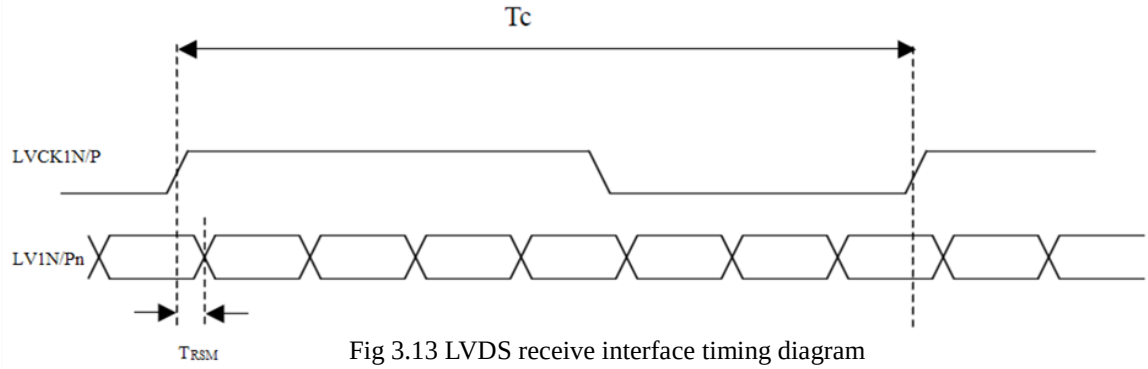


Fig 3.13 LVDS receive interface timing diagram

3.4 Power On/Off Sequence

The power sequence specifications are shown as the following table and diagram

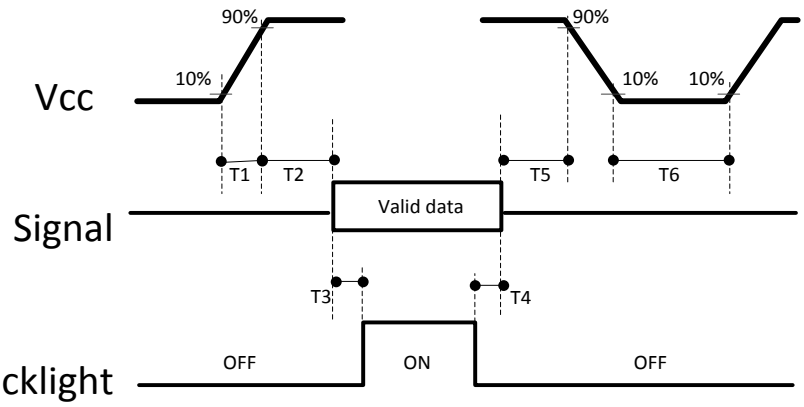


Fig 3.14 Power on/off signal sequence

Parameters	Values			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	500	-	-	ms
T4	100	-	-	ms
T5	0	-	50	ms
T6	1000	-	-	ms

Attention:

(1) The supply voltage of the external system for the module input should be the same as the definition.

(2) To avoid some abnormal display noise, we suggest " VCC falling time" to follow "T6" definition.

(3) The product should be always operated within above ranges.

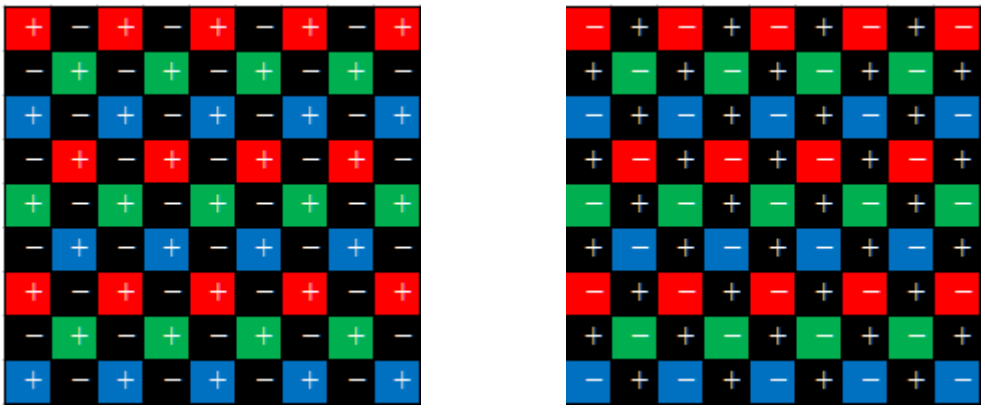
(4) In case of VCC is off level, please keep the level of input signals on the low or keep high impedance.

3.5 Flicker Adjustment

Flicker must be optimized after module assembly and aging. Its patterns are as follow:

Dot On/Off sub pixel checker under 50% gray level.

Sub pixel checker 128 gray



Frame N Fig 3.15 Flicker pattern Frame N+1

3.6 Driver IC ESD Specification

If the LCD module is designed with the plastic bezel, we suggest ESD protection solutions should be applied to avoid IC damaged, as shown in Fig.3.16.

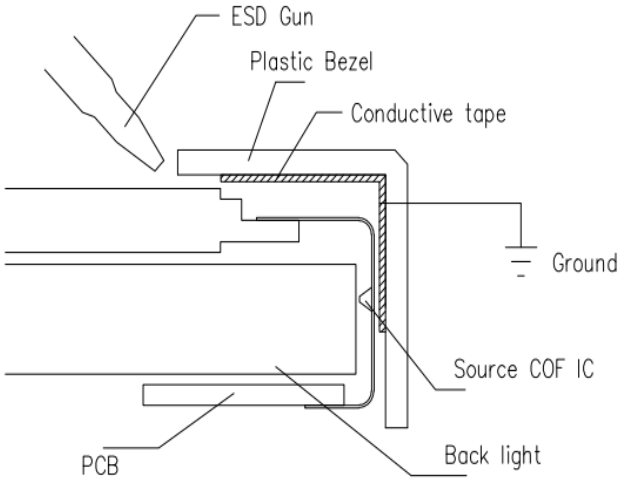


Fig. 3.16 Source COF IC ESD protection

4. OPTICAL CHARACTERISTICS

4.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25±2	℃
Ambient Humidity	H_A	50±10	% RH
Supply Voltage	V_{CC}	12	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	F_v	60	Hz
Light source	HKC 31.5" WXGA module White LED Backlight Module/ Film structure		
Warm up time	Twarm	>30 min	min
Dark room	ED	1lux>	lux

To avoid abrupt temperature change during optical measurement, the measurement should be executed in a stable, windless, in dark room after lighting the light source.

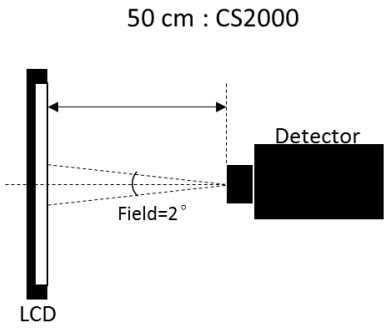


Fig 4.1 Measurement equipment.

4.2 Optical Specifications

The relative measurement methods of optical characteristics are shown in 4.2. The following items should be measured under the test conditions described in 4.1 and stable environment shown in 4.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity (CIE1931)	Red	Rx	θ_x=0°,θ_y=0 ° Viewing Angle at Normal Direction at center point of panel, Light source is HKC Backlight	Typ - 0.03	(0.632)	Typ + 0.03	--	(1)
		Ry			(0.331)			
	Green	Gx			(0.309)			
		Gy			(0.595)			
	Blue	Bx			(0.152)			
		By			(0.050)			
	White	Wx			(0.279)			
		Wy			(0.278)			
Color Gamut		CG		65	68		%	(2)
Transmittance		T%		-	5.5		%	(3)
Contrast Ratio		CR	θ_x=0°,θ_y=0 °	-	3000		-	(4)
Response Time		T_g		-	8.5	17	ms	(5)
Viewing Angle	Horizontal	θ_x+	CR≧10	-	89	-	Deg.	(6)
		θ_x -		-	89	-		
	Vertical	θ_y+		-	89	-		
		θ_y-		-	89	-		

Note:

(1) Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying (Red, Green, Blue, White) and light source is defined by HKC Backlight, Measurements shall be made at the center of the panel, and setup of measurement is shown in Fig 4.1.

(2) The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1931 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig 4.1.

(3) Definition of Transmittance (T%):

The transmittance is measured with full white pattern (Lmax) at the center of the LCD panel.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}}$$

(4) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression,

Contrast Ratio (CR): $\boldsymbol{CR} = \frac{\boldsymbol{CR_W}}{\boldsymbol{CR_D}}$

CRW : Luminance of LCD module with full screen white pattern (255,255, 255) at center point.

CRD : Luminance of LCD module with full screen dark pattern (0, 0, 0) at center point.

Where the measure point of to the Contrast Ratio is the center of the panel

(5) Definition of Response time (Tg):

Average of gray to gray response time (Tg) means the average switching time of luminance ratios among 0%,25%,50%,75%,and 100% to each other and is optimized on frame rate =60Hz.

Measured Response time		To				
		0%	25%	50%	75%	100%
From	0%		$T_{0\%to25\%}$	$T_{0\% to 50\%}$	$T_{0\% to 75\%}$	$T_{0\% to 100\%}$
	25%	$T_{25\% to 0\%}$		$T_{25\% to 50\%}$	$T_{25\% to 75\%}$	$T_{25\% to 100\%}$
	50%	$T_{50\% to 0\%}$	$T_{50\% to 25\%}$		$T_{50\% to 75\%}$	$T_{50\% to 100\%}$
	75%	$T_{75\% to 0\%}$	$T_{75\% to 25\%}$	$T_{75\% to 50\%}$		$T_{75\% to 100\%}$
	100%	$T_{100\% to 0\%}$	$T_{100\% to 0\%}$	$T_{100\% to 50\%}$	$T_{100\% to 75\%}$	

Table 4.2 Switching time of luminance ratios matrix

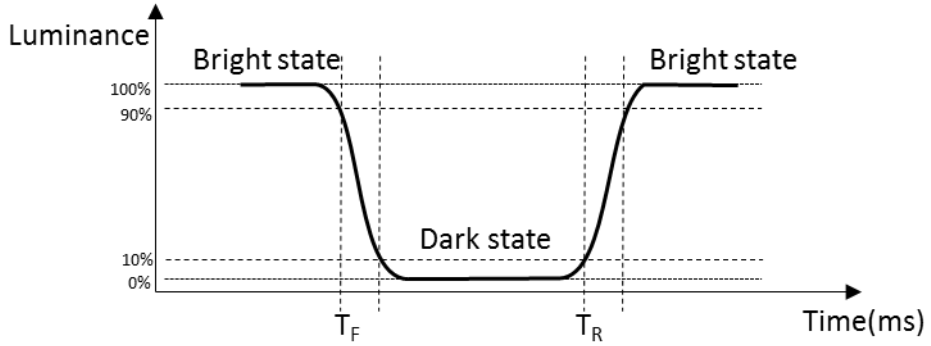


Fig 4.3 The definition of TR and TF

Measured response time is determined by 10% to 90% brightness difference of rising (TR) or falling (TF) time.

(6) Definition of Viewing angle:

As Note (4) the static contrast ratio definition, the viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the HKC's module (two vertical angles: up θy+ and down θy-; and two horizontal angles: right θx+ and left θx-). The standard setup of measurement is shown in Fig 4.1 & 4.4

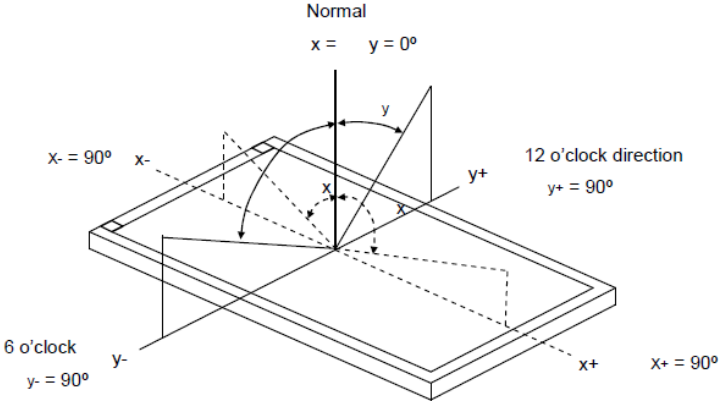
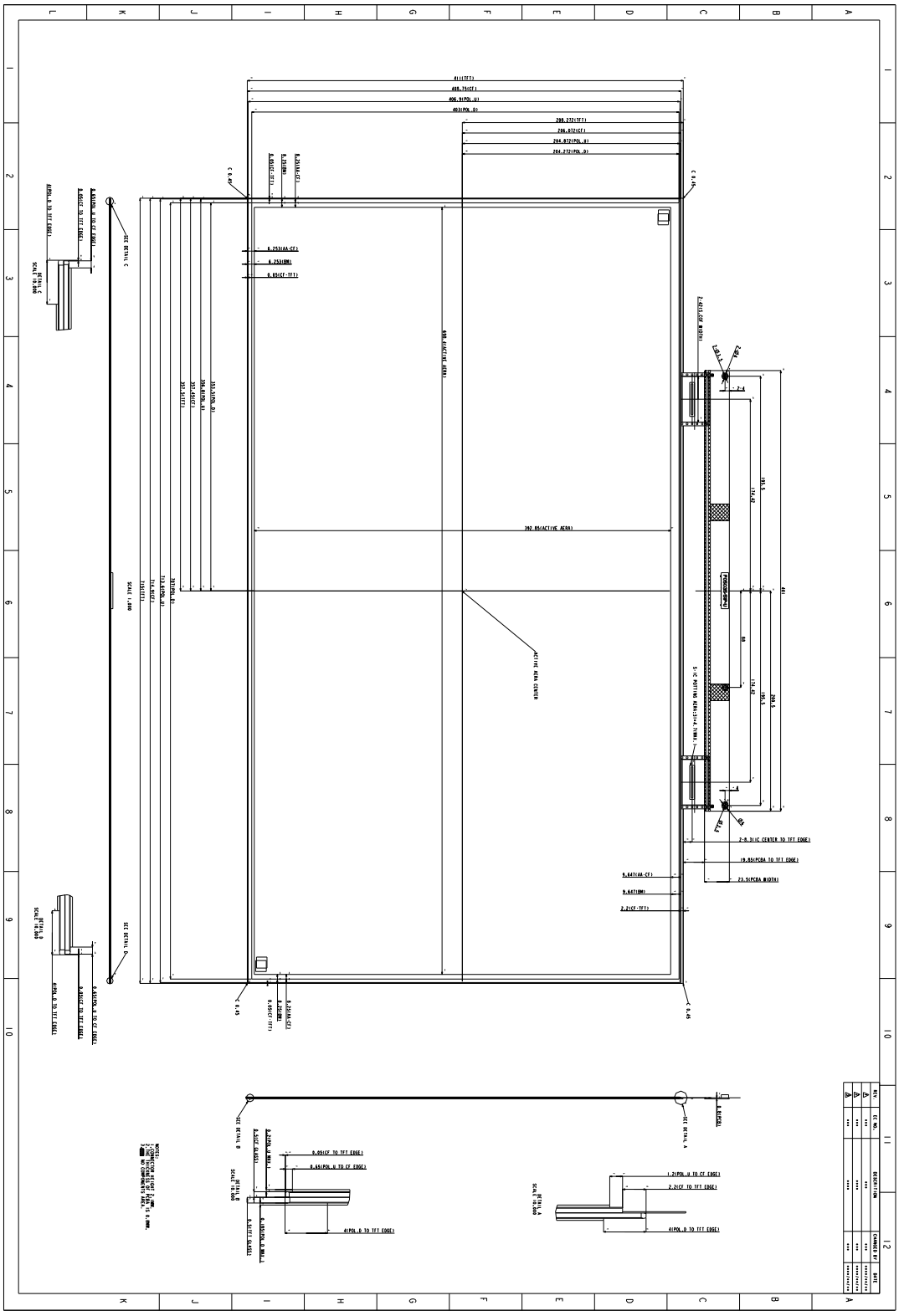


Fig 4.4 The measurement of viewing angle

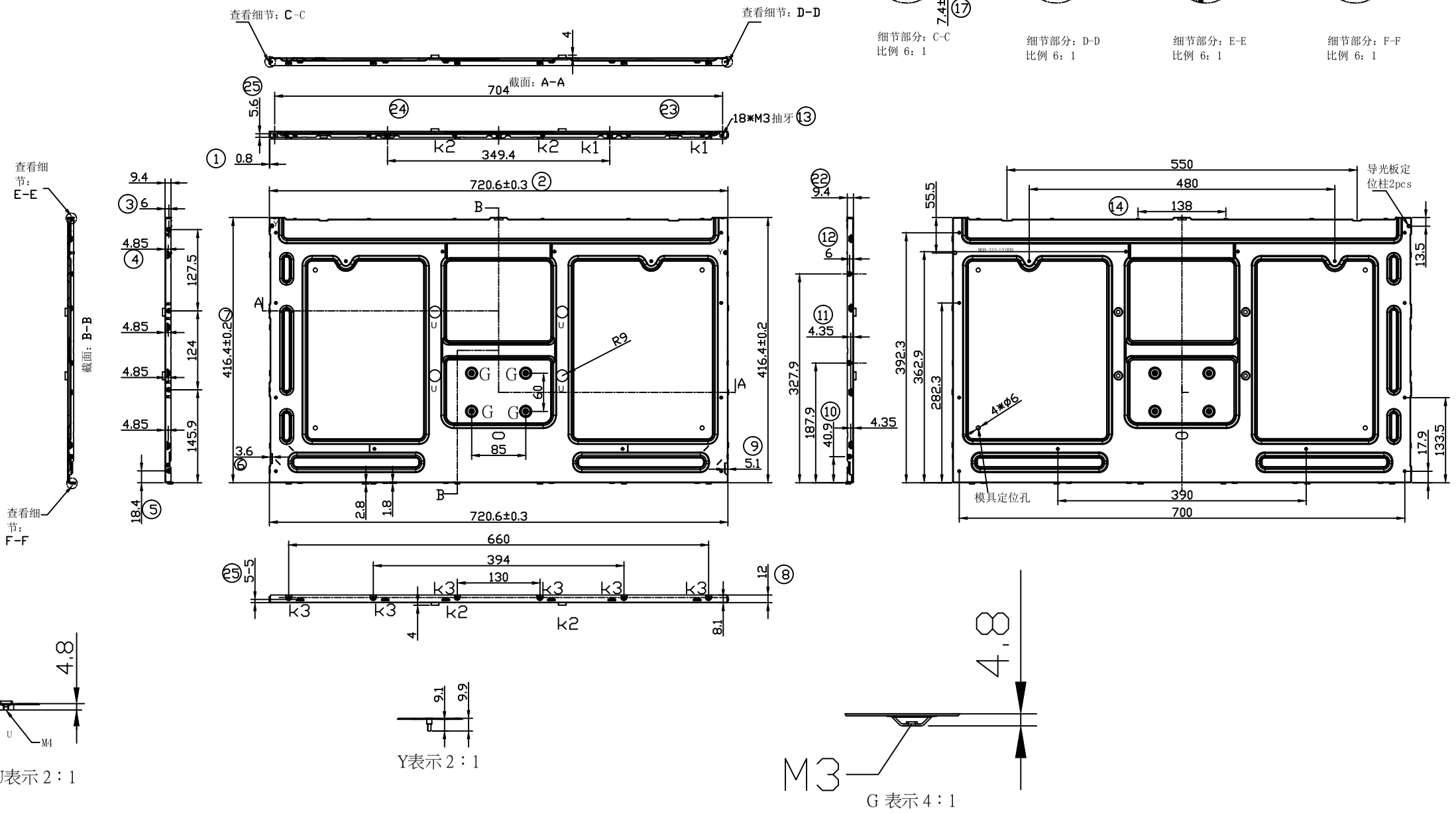
5. MECHANICAL CHARACTERISTICS

5.1 Mechanical Specification



CLASS / LIMITS	f	m	c	v
0.5~6	±0.05	±0.1	±0.2	±0.3
>6~30	±0.10	±0.2	±0.3	±0.5
>30~120	±0.15	±0.3	±0.8	±1.5
>120~400	±0.2	±0.5	±1.2	±2.5
>400~1000	±0.3	±0.8	±2	±4
>1000~2000	±0.5	±1.2	±3	±6

序号	标记	更改内容	日期	署名
0	△0	首次发行		



细节部分：C-C
比例 6：1

细节部分：D-D
比例 6：1

细节部分：E-E
比例 6：1

细节部分：F-F
比例 6：1

零件规格/用量表				
序号	规 格	料 号	用量	备注
1	φ12*φ10*L6.1*M4		4	
2				
3				
4				
5				
6				

技术要求：

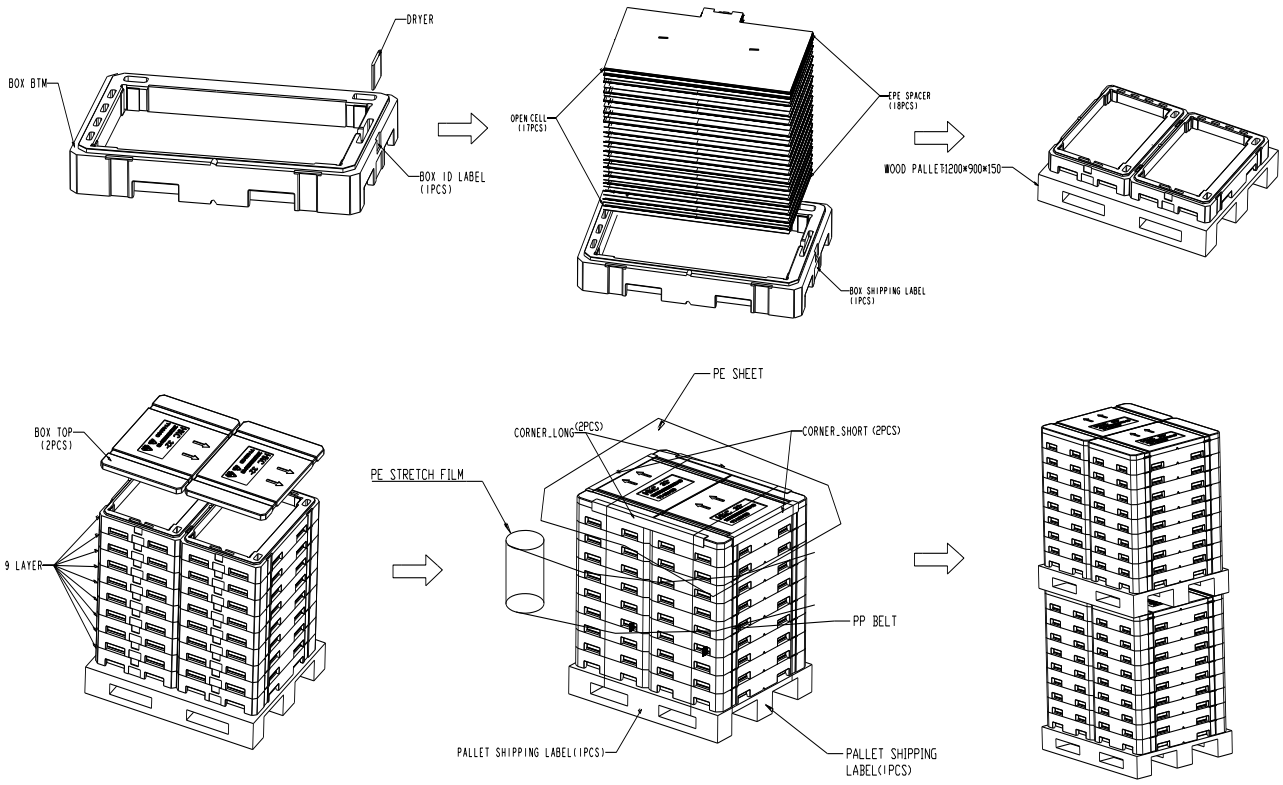
1，材质：SGCC，T=0.8
2，表面无刮伤，油污，锈斑，翘曲变形（毛刺高度小于0.03MM）
3，抽牙孔不能有破损，不平现象
4，侧面卡勾端面平整，不可倾斜
5，反射片装配面平整度管控在内凸0.3，外凹1MM范围内
6，未注圆角R=1.0，内直角≤0.2°，未注公差请按F级别管控
7，产品采用无尘包装

四个4mm壁挂+4个凸包背板

5.2 Packing

5.2.1 Packing Specifications

Item	Specification		
	Quantity	Dimension (mm)	Weight (kg)
Packing Box	17pcs/box	857(L) x 558(W) x 105(H)	Net Weight: TBD Gross Weight: TBD
Pallet	1	1200(L) x 900(W) x 150 (H)	Net Weight: 16.5Kg
Stack Layer	9		
Boxes per Pallet	18		
Pallet after Packing	306pcs/pallet	1200(L) x 900(W) x 1074.5(H)	Gross Weight: TBD



6. DEFINITION OF LABELS

6.1 Open Cell Label

TBD

7. PRECAUTION

Please pay attention to the followings when a TFT-LCD cell is used, handled and mounted.

7.1 Unpacking

Should use immediately after unpacking TFT-LCD cell to prevent the terminal corrosion.

Protection film for a polarizer on a TFT open cell should be slowly peeled off so that the electrostatic charge can be minimized.

Source PCB should be connected to the ground when peel off the protection film.

The protection film should not be contacted to the driver during peeling off.